

Starlord KBL Refresh Schematics KabyLake-R


2017-05-25

REV : A00

DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

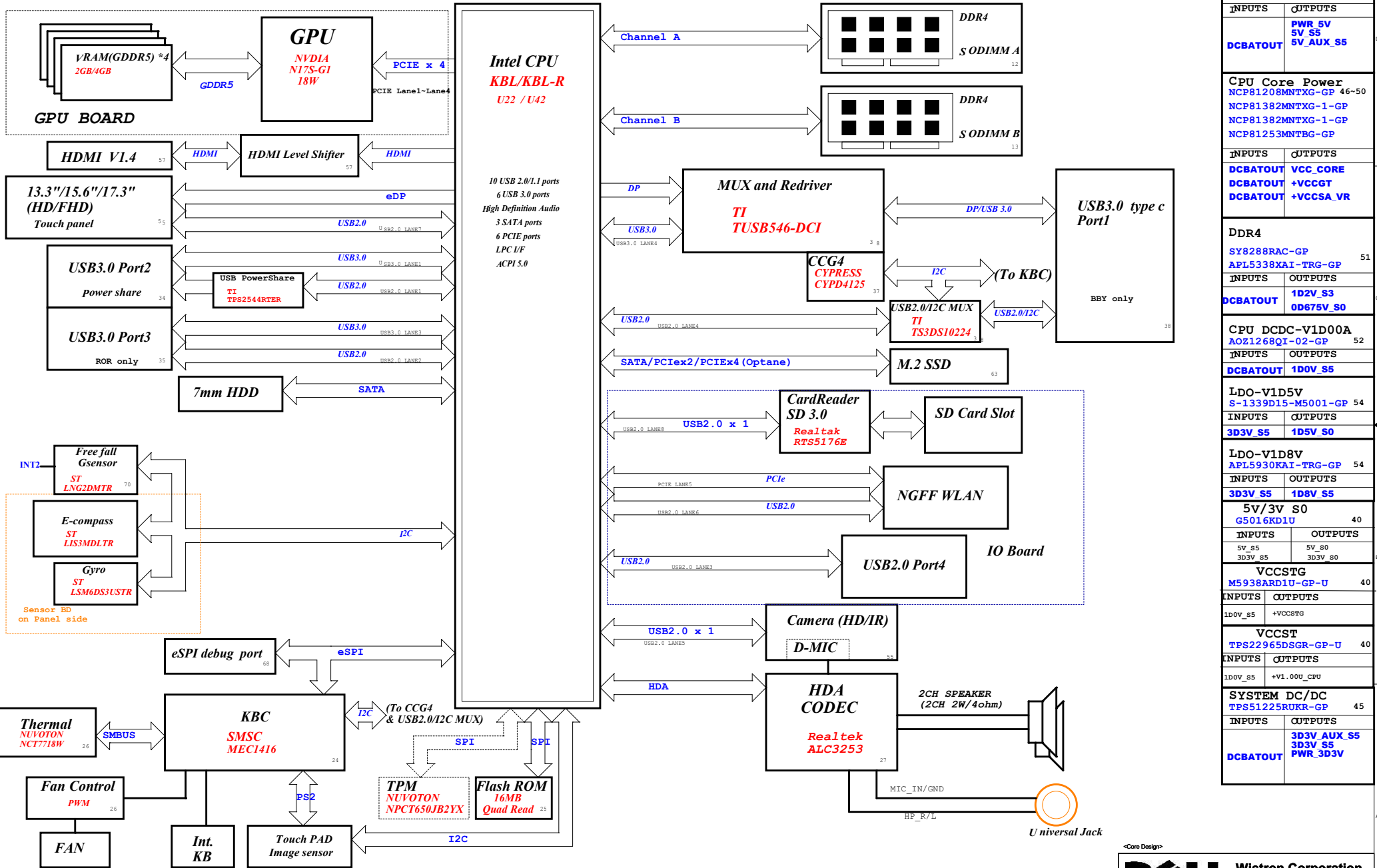
<Core Design>		
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Title		
Cover Page		
Size A 3	Document Number Starlord KBL-R	Rev A 00
Date: Monday, August 28, 2017	Sheet 1	of 106

Project code: 4PD0CF010001(SL13_R)
4PD0CG010001(SL15_R)
4PD0CH010001(SL17_B)

PCB P/N: 16888
Revision: A00

Star lord KBL Block Diagram

	SENSOR	IO	MB
ROR	17A18-SA	17A17-SA	17810-1
BBY	17A18-SA	17A16-SA	16888-1



CHARGER ISL88739		44
INPUTS	OUTPUTS	
AD+	DCBATOUT	
BT+		
SYSTEM DC/DC SY8288CRAC-GP		45
INPUTS	OUTPUTS	
DCBATOUT	PWR 5V 5V_S5 5V_AUX_S5	
CPU Core Power NCP81208MNTXG-GP		46-50
NCP81382MNTXG-1-GP		
NCP81382MNTXG-1-GP		
NCP81253MNTBG-GP		
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
DCBATOUT	+VCCGT	
DCBATOUT	+VCCSA_VR	
DDR4 SY8288RAC-GP		51
APL5338XAI-TRG-GP		
INPUTS	OUTPUTS	
DCBATOUT	1D2V_S3 0D675V_S0	
CPU DCDC-V1D00A AOZ1268Q1-02-GP		52
INPUTS	OUTPUTS	
DCBATOUT	1D0V_S5	
LDO-V1D5V S-1339D15-M5001-GP		54
INPUTS	OUTPUTS	
3D3V_S5	1D5V_S0	
LDO-V1D8V APL5930KAI-TRG-GP		54
INPUTS	OUTPUTS	
3D3V_S5	1D8V_S5	
5V/3V S0 G5016KD1U		40
INPUTS	OUTPUTS	
5V_S5 3D3V_S5	5V_S0 3D3V_S0	
VCCSTG M5938ARD1U-GP-U		40
INPUTS	OUTPUTS	
1D0V_S5	+VCCSTG	
VCCST TPS22965DSGR-GP-U		40
INPUTS	OUTPUTS	
1D0V_S5	+V1.00V_CPU	
SYSTEM DC/DC TPS51225RUKR-GP		45
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5 3D3V_S5 PWR_3D3V	

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File: **Block Diagram**

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SSID = CPU

(Blanking)

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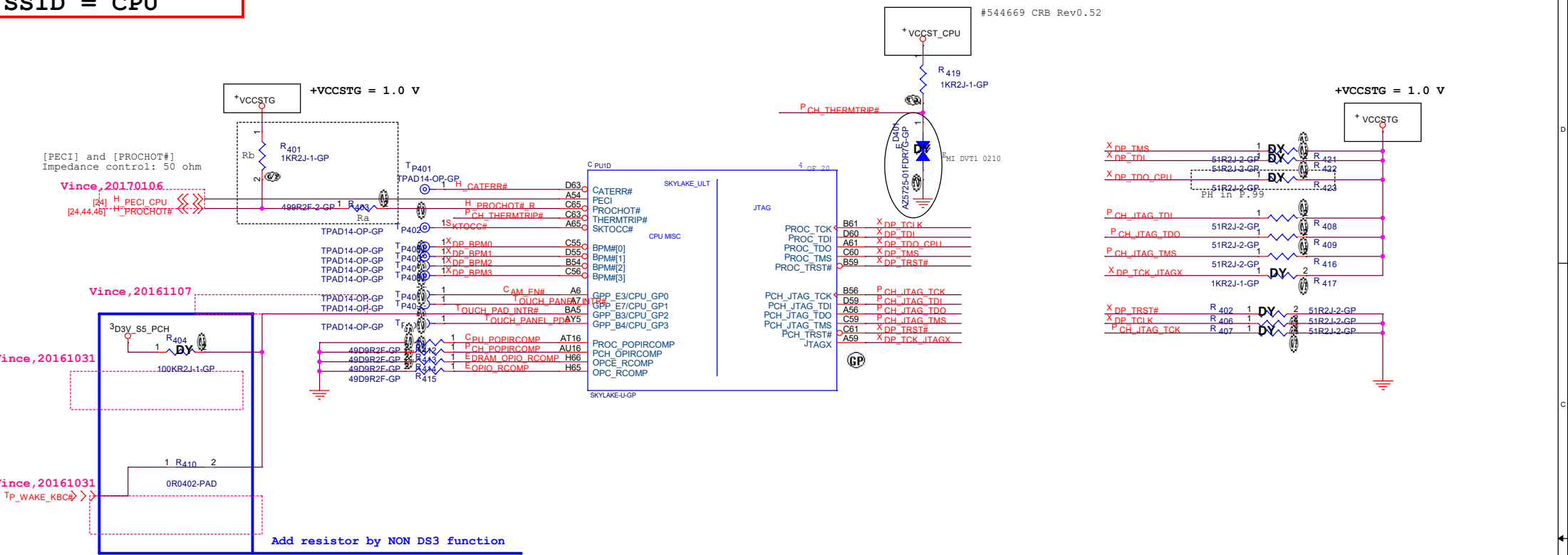
Starlord KBL-R

Rev

A00

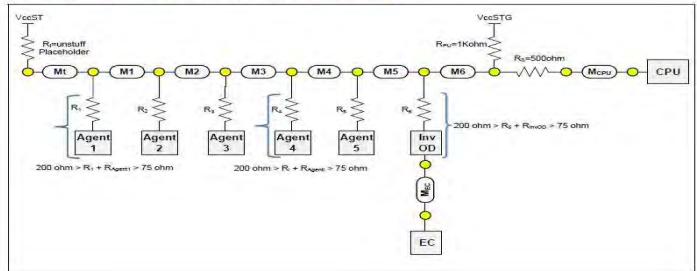
Date: Monday, August 28, 2017Sheet 3 of 106

SSID = CPU



(#543016) PROCHOT# Routing Guidelines

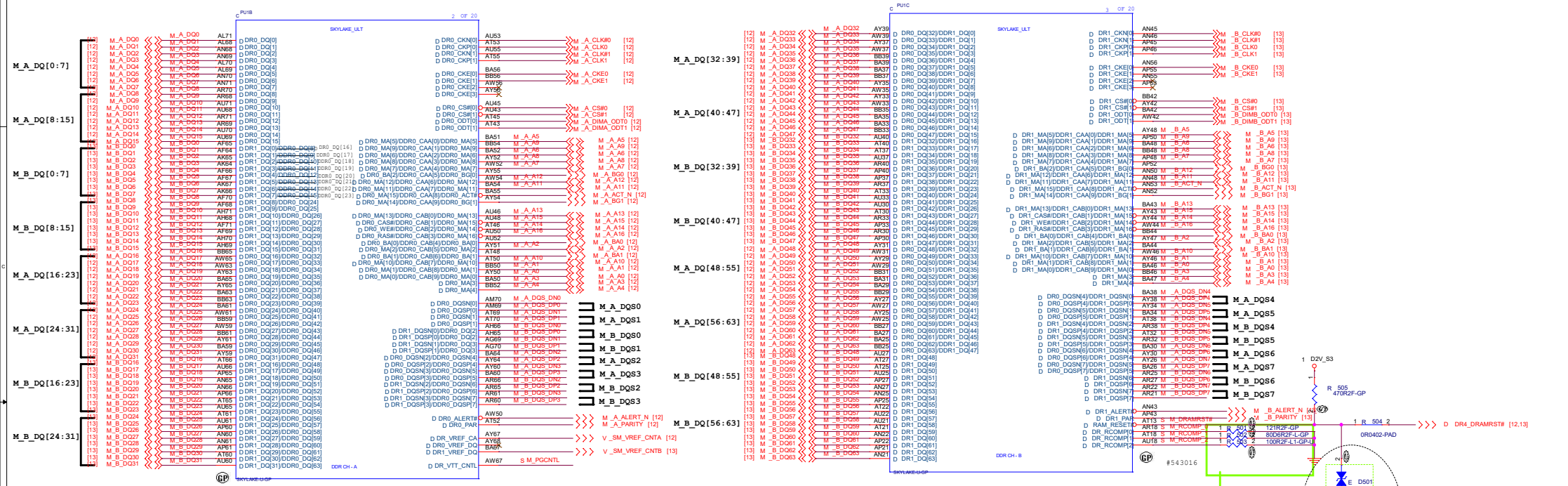
Figure 10-1. Routing Illustration for PROCHOT# Topology

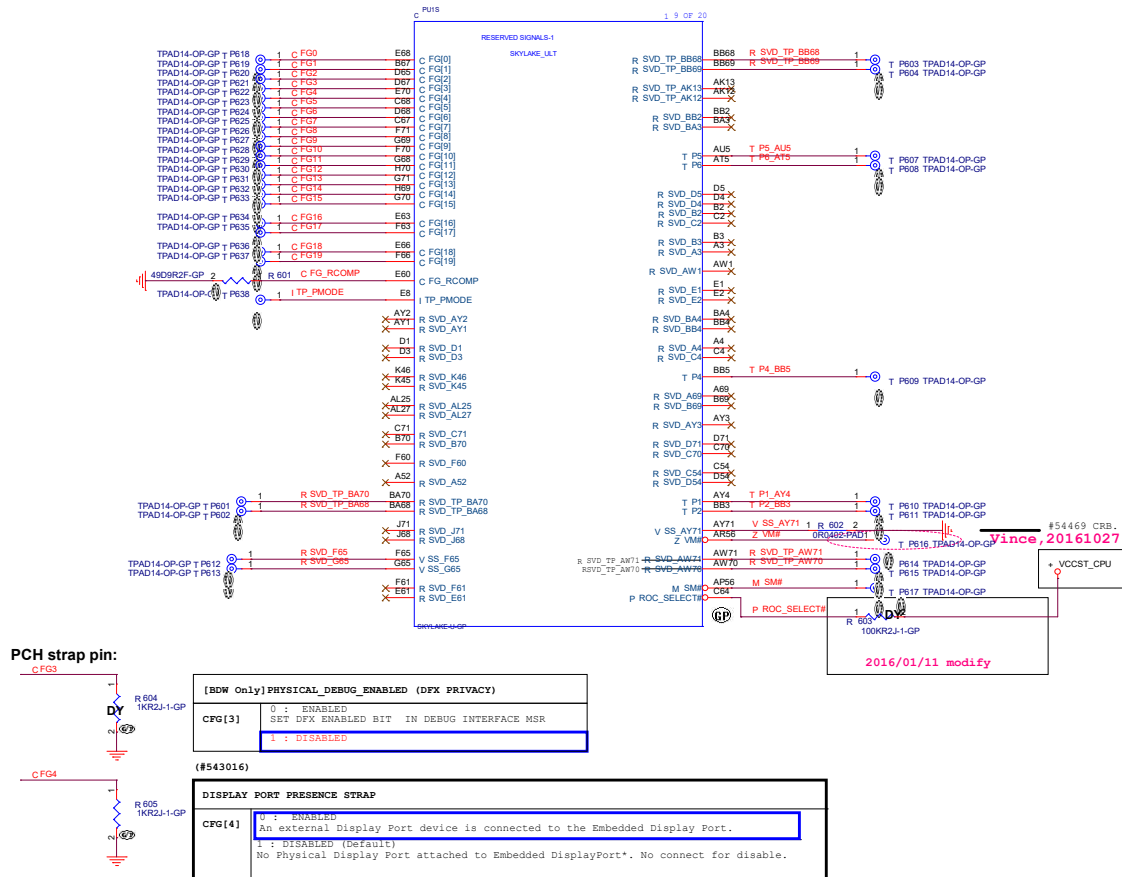


M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route (M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

SSID = CPU

DDR4 ball type: Interleaved Type

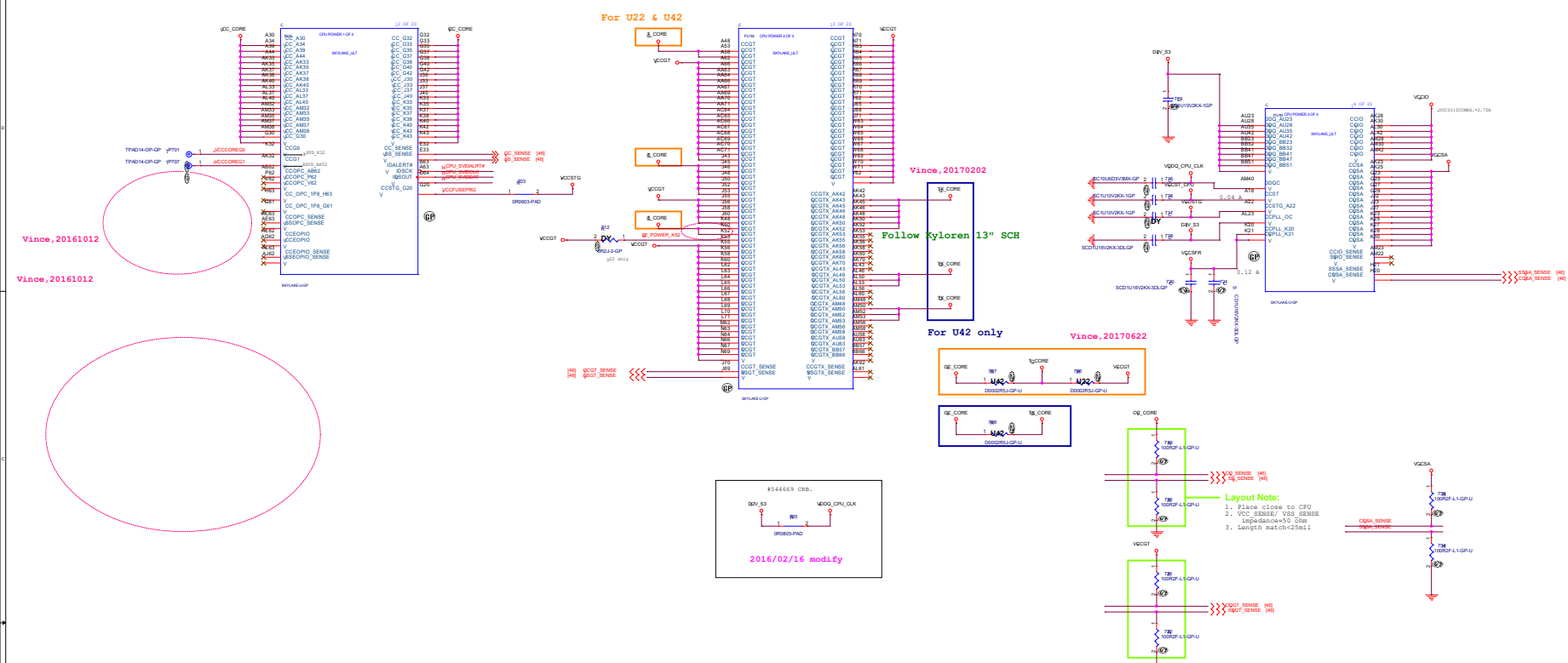




SKL (#543016) :

Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

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SVID DATA

Layout Note:
The total length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.



SVID CLOCK

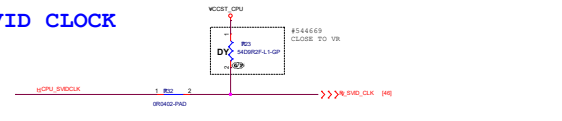


Figure 10-7. Routing Illustration for SVID Topology

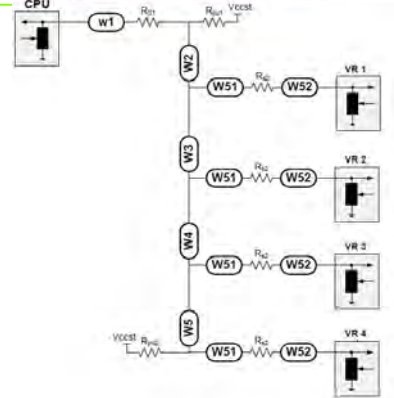
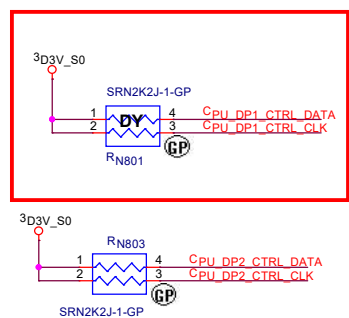


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [mil/inch]	W2 [mil/inch]	W3/4/5 [mil/inch]	W2+W3+W4+W5 [mil/inch]	W3 [mil/inch]	W2 [mil/inch]	R _{term} [Ω]	R _{pull} [Ω]	R ₁ [Ω]	R ₂ [Ω]	V _{CE} [V]
VIDOUT							100	100	0	10	
VIDSCK	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50	1.0
VIDALERT							56	Empty	220	0	

SSID = CPU

Dummy, Vendor suggest
20141117

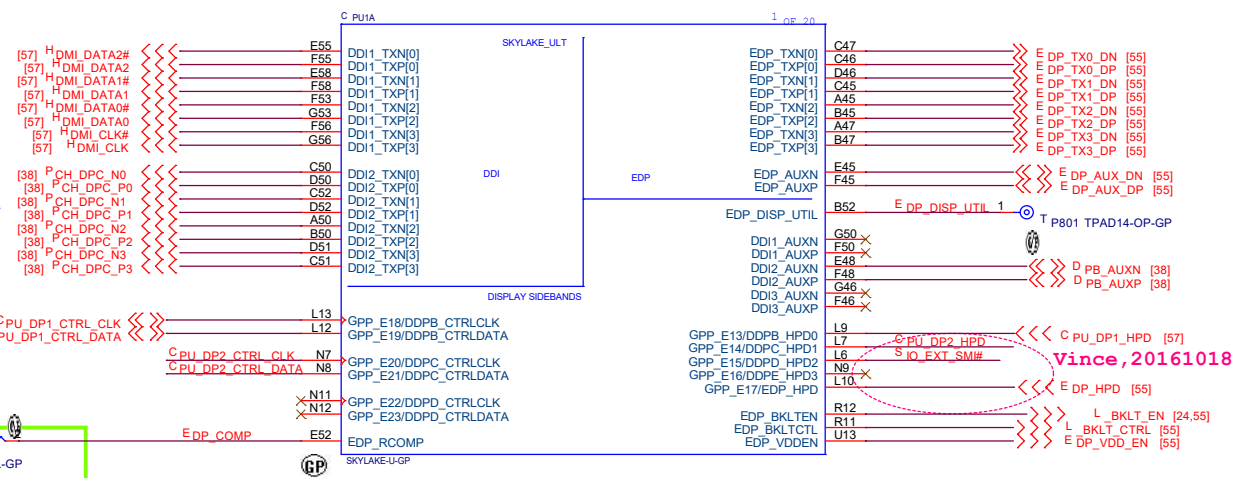
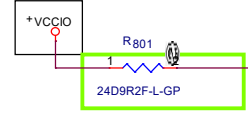


HDMI

DP and DP to VGA

HDMI

Check



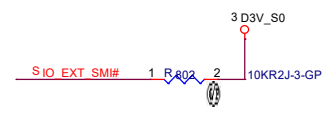
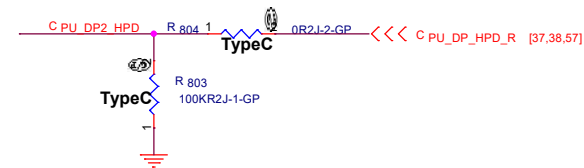
(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω \pm 1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC



Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 Ω \pm 1% resistor.

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Title: **CPU (DISPLAY)**

Size: A3 Document Number: **Starlord KBL-R** Rev: **A00**

Date: Friday, December 08, 2017 Sheet: 8 of 106

Main Func = CPU

(Blanking)

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Title

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Size

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Document Number

Starlord KBL-R

Rev

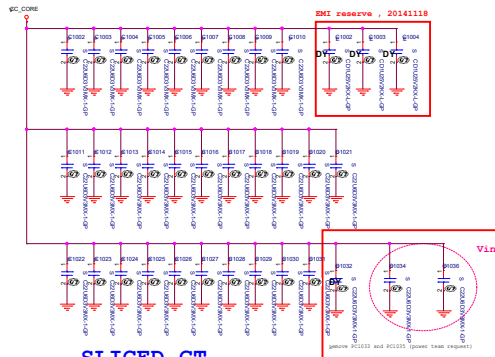
A00

Date: Monday, August 28, 2017

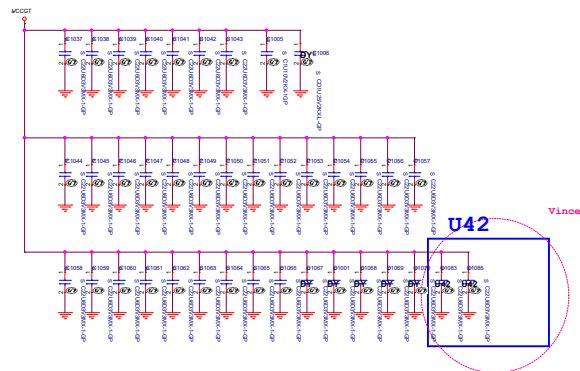
Sheet 9 of 106

For U42

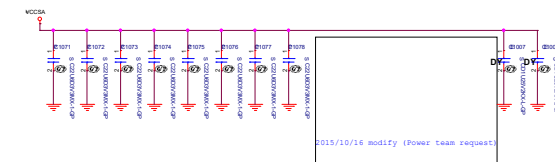
EMI reserve , 20141118



U-line 23e 28W
IccMax current-10ms max[A] = 67 A
22U 0603 x35 (5 DY)



22U 0603 x13 (5 DY)



Initial Operating Conditions	Requirements	Notes
VCC1 Power Plane at VBI output	1x 220µF (0.4-5mΩ ESR) 1x 220µF (0.4-5mΩ ESR)	Placed at primary side near to VBI output Placed at backside side near to VBI output
VCC2 Power Plane at VR output	2x 220µF (0.4-5mΩ ESR) 1x 220µF (0.4-5mΩ ESR)	Placed at primary side near to VR output Placed at primary side near to VBI output
VCC3 Power Plane at VR output	1x 220µF (0.4-5mΩ ESR)	Additional components needed when supplying 23A
VCC4 Power Plane at VR output	1x 220µF (0.4-5mΩ ESR)	Placed at primary side near to VR output Only needed when supplying 23A
VCC5 Power Plane at VR output	2x 220µF (0.4-5mΩ ESR)	Placed at primary side near to VR output
VCC6 Power Plane at VR output	2x 47µF 680V	Placed at primary side near to VR output
VCC7 Power Plane at VR output	2x 47µF 680V	Placed at primary side near to VR output

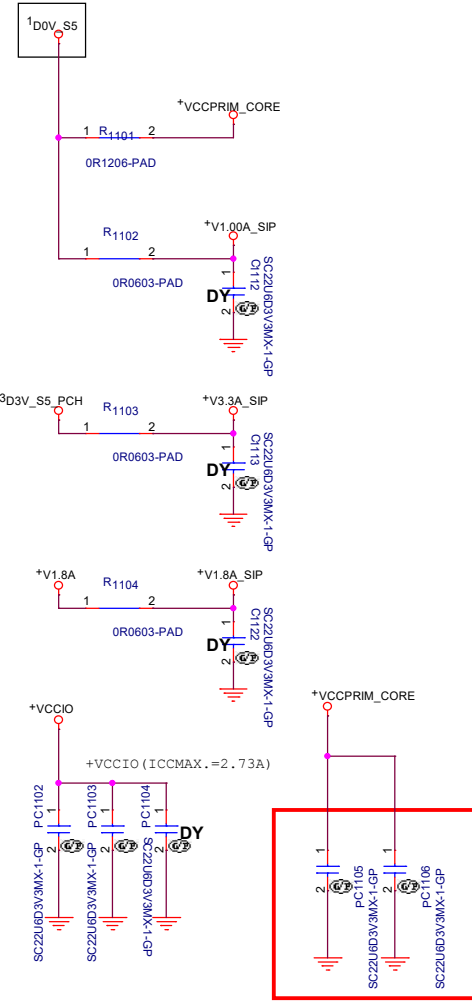
Table S3-4. Decoupling Requirements for SKI U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placed on guideline
VOC	5x 22uF 0603 7x 10uF 0402 25x 1uF 0201	5x 47uF 0905 (6.3V) 8x 10uF 0402	Place on secondary side, underneath the package Place as close to the package as possible
VOCOT	15x 10uF 0402 12x 1uF 0201	3x 47uF 0905 (6.3V) 7x 22uF 0603 3x 47uF 0909 5x 22uF 0603	Place on secondary side, underneath the package Place as close to the package as possible Additional components needed when supporting 23V
VOCOT1	8x 10uF 0402	8x 22uF 0603	Place on secondary side, underneath the package Only needed when supporting 23V
VOC5A	7x 10uF 0402 7x 1uF 0201	8x 10uF 0402	Place on secondary side, underneath the package Place as close to the package as possible
VOCQ1	2x 10uF 0402 4x 1uF 0201	4x 1uF 0402	Place on secondary side, underneath the package Place as close to the package as possible
VOCQ2	2x 10uF 0402 4x 1uF 0201	4x 10uF 0402	Place on secondary side, underneath the package Place as close to the package as possible
VOCQ3	1x 1uF 0201	3x 1uF 0402	Place on secondary side, underneath the package Place as close to the package as possible
VOCST		1x 1uF 0402	Place as close to the package as possible

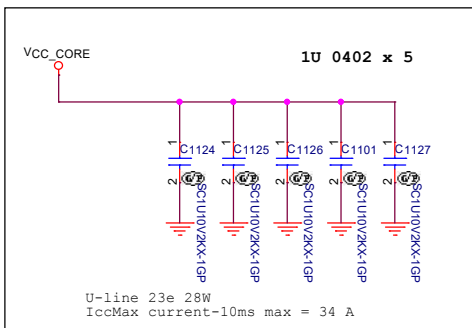
Domain	Backside cap	Primary side cap	Ejectment guideline
VCC3T0	1x 10µF 0402		Place on secondary side, underneath the package Backside only
VCCOP02	2x 10µF 0402		Place on secondary side, underneath the package
VCCOP0	1x 10µF 0402 8x 1µF 0201		Place on secondary side, underneath the package

Main Func = CPU

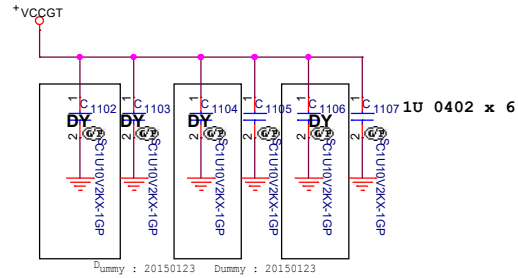
PCH DERIVED RAILS



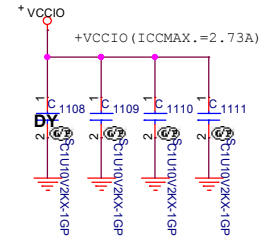
Size:0805 change to 0603
20141117



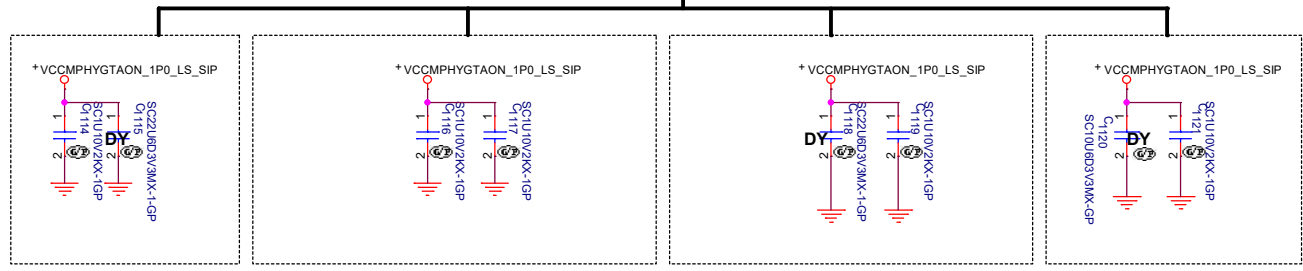
UNSLICED GT



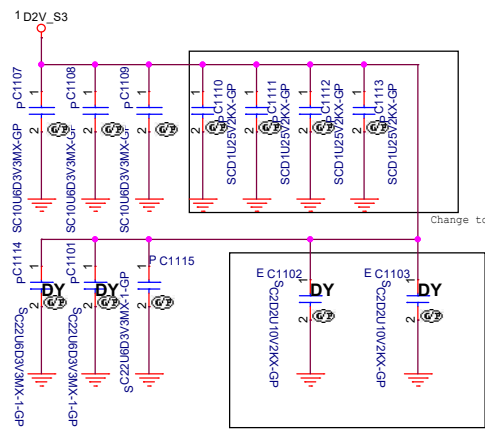
VCCIO



+VCCMPHYGTAON_1P0 (ICCMAX.=2.12A)



Layout Note:
1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15



Change to 0.1uF at 20150427 for Power team

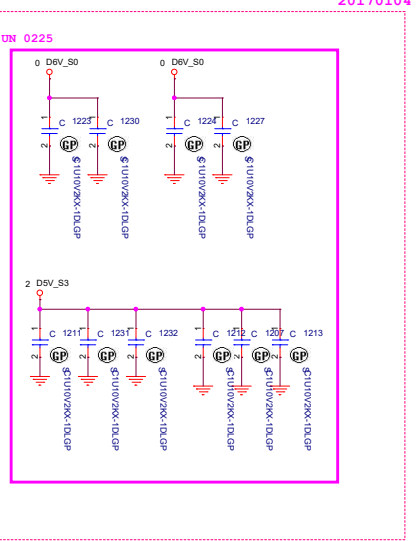
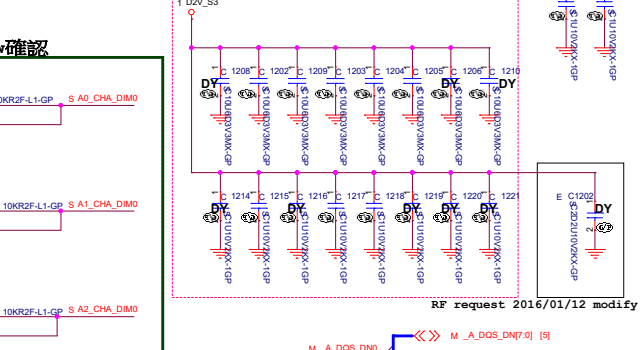
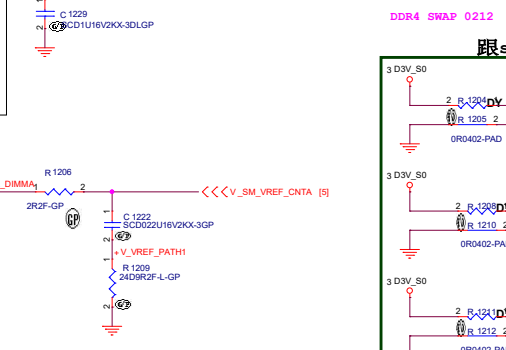
RF request 2016/01/12 modify

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Title: **CPU (Power CAP2)**

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Title (Reserved)_SODIMM _SODIMM4					
Size A4		Document Number Starlord KBL-R			Rev A 00
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Main Func = PCH

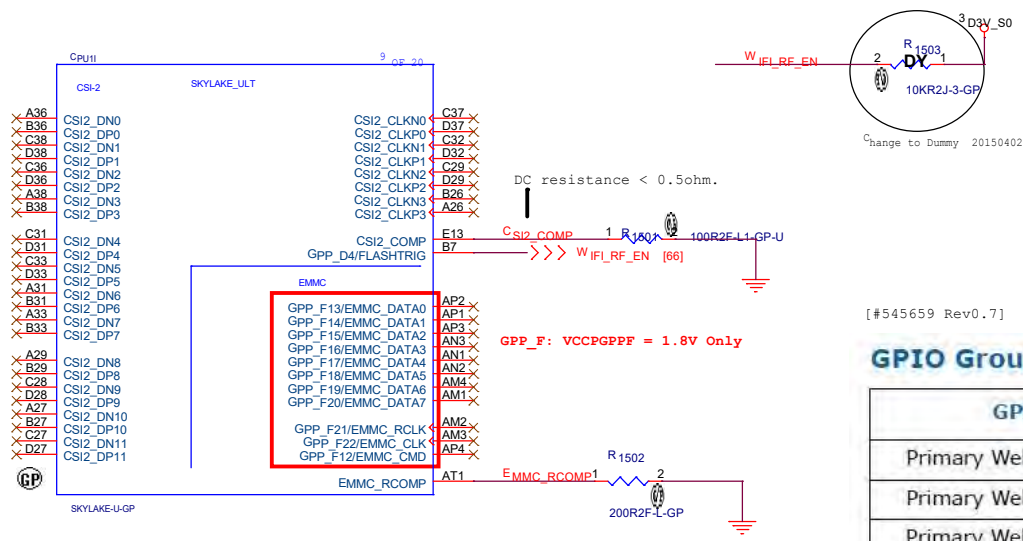


Table 8-1. Switchable Graphics GPIO Requirements


GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH, It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSENT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

[#545659 Rev0.7]

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

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Title

CPU (CS-2/EMMC)

Size
A 3

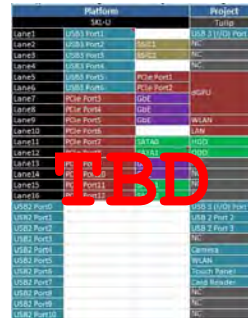
Document Number

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A00

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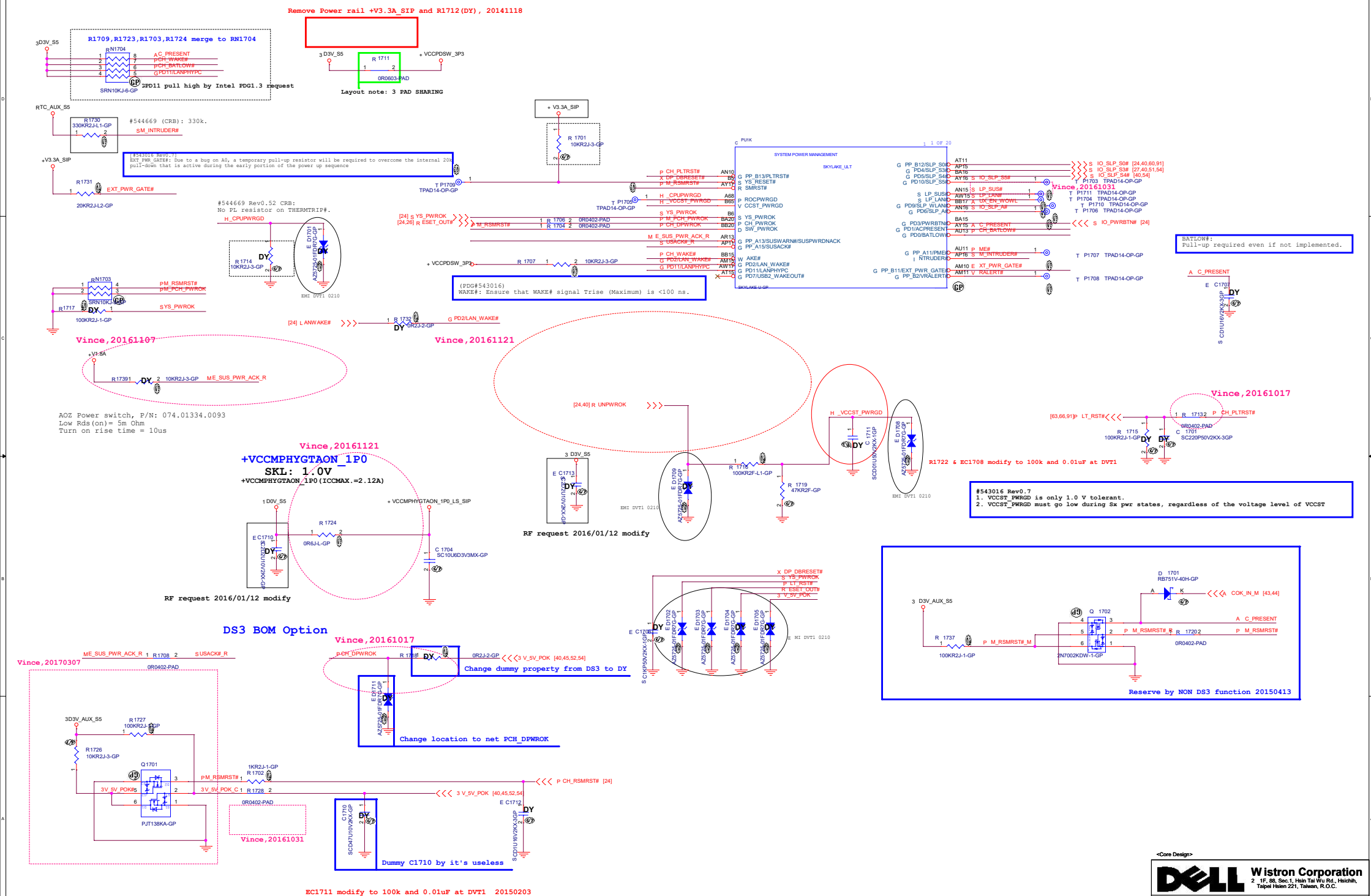
SKU	Max Device (Ports)	Max Lanes	PCIe+ Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

SRL	PCIe Link Config	PCI Express® Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
	1x4	Port1				Port5							
Y	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8				
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

16	PCIE #12	SATA #2	X4	X2	Inter PCIe Storage Device #3
15	PCIE #11	SATA #1			
14	PCIE #10	GBE	X4	X2	Inter PCIe Storage Device #2
13	PCIE #9	GBE			
12	PCIE #8	SATA #1	X2	X2	Inter PCIe Storage Device #1
11	PCIE #7	SATA #0			
10	PCIE #6	GBE	X2	X2	
9	PCIE #5	GBE			
8	PCIE #4	GBE	X2	X2	
7	PCIE #3	GBE			
6	PCIE #2		X4	X2	
5	PCIE #1				
4	USB3 #4		X2	X2	
3	USB3 #3				
2	USB3 #2	SSIC #1	X2	X2	
1	USB3 #1 (Capable of OTG)				

[illegible]

5
Main Func = PCH



SSID = PCH

PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC.

This signal has a weak internal pull-down.

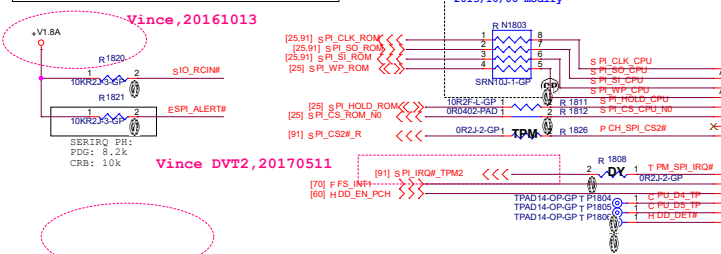
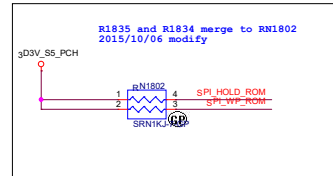
This signal has a weak internal pull-down.

PCH strap pin:

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

This signal has a weak internal pull-up



Vince DVT2,20170511

Vince, 20161017

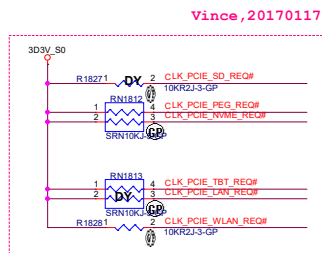
RCIN#:
Frequency to Avoid: 33 MHz

Vince, 2016-2017

Vince, 20161013



Vince, 20161017



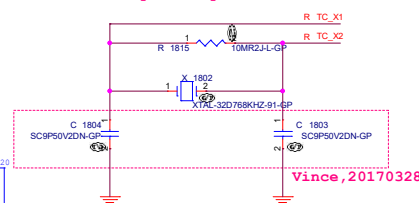
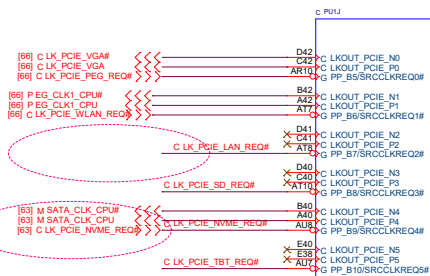
Vince,20170117

Vince, 20161026

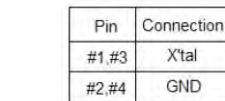
Vince, 20161026

WLAN

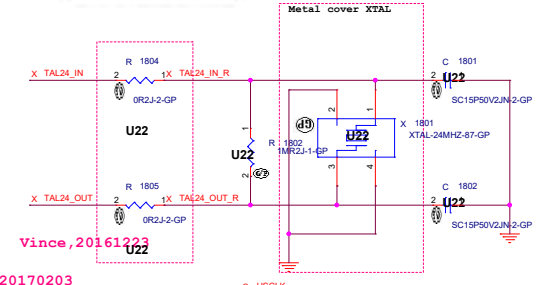
SSD



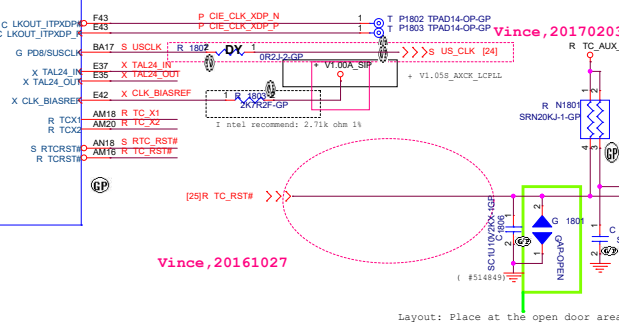
Vince, 20170328



Vince,20170110



Vince, 2016122



Vince, 20161027

Layout: Place at the open door area.

<Core Design>



Title		
CPU (LPC/SPI/SMBUS/CL/CLK)		
Size A 2	Document Number	Rev A 00
S tarlord KBL-R		
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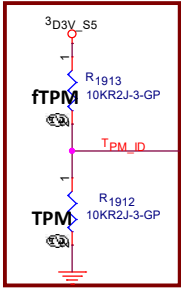
SSID = PCH

Strap pin:

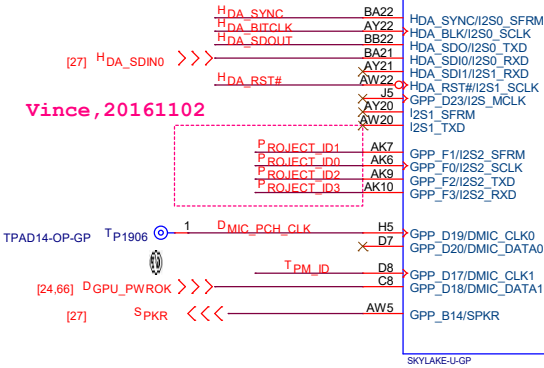
Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. ★ 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. ★ 1 = Port C is detected.

These two signals have weak internal pull-down.

Vince,20161107



Vince,20161102



PCH strap pin:

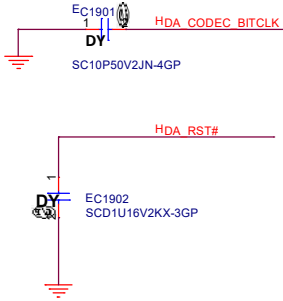
Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default ★ High = Enable

The internal pull-down is disabled after PLTRST# deasserts

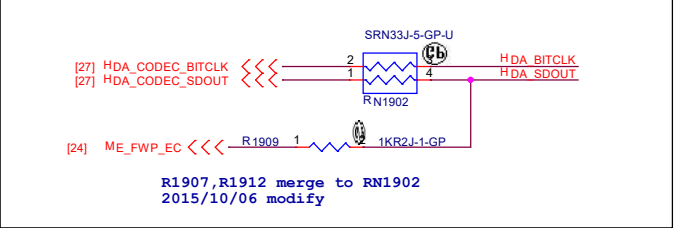
PCH strap pin:

NO REBOOT	
HDA_SPKR	★ Low = Enable (Default) High = Disable

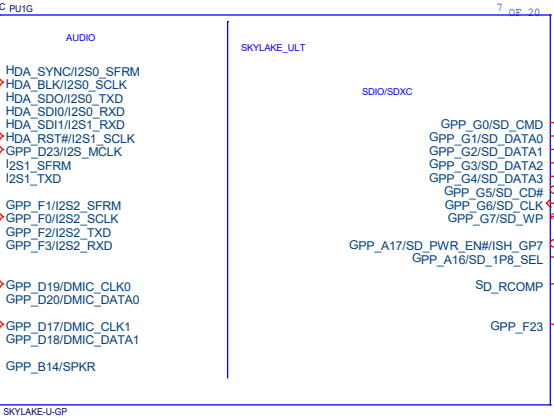
The internal pull-down is disabled after PLTRST# deasserts



Vince,20170106

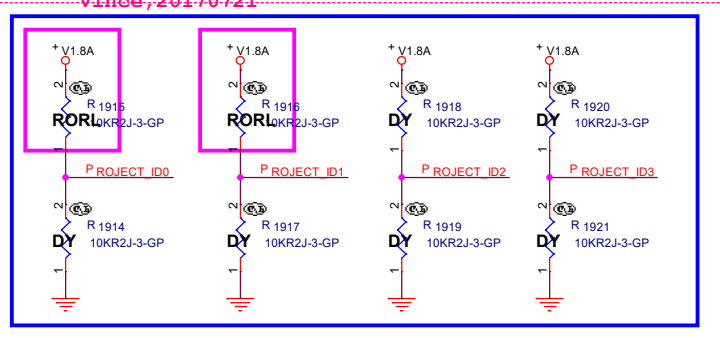


R1907,R1912 merge to RN1902
2015/10/06 modify



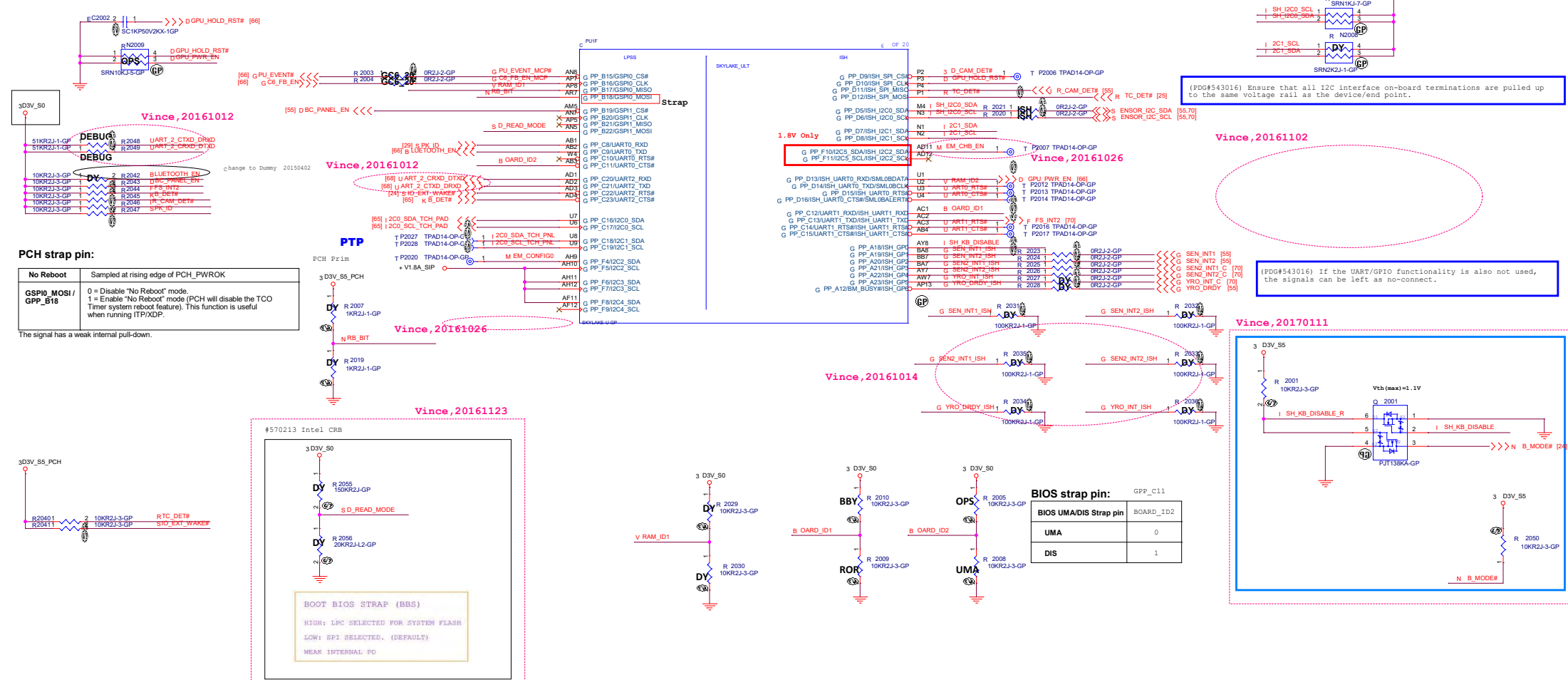
Vince,20170721

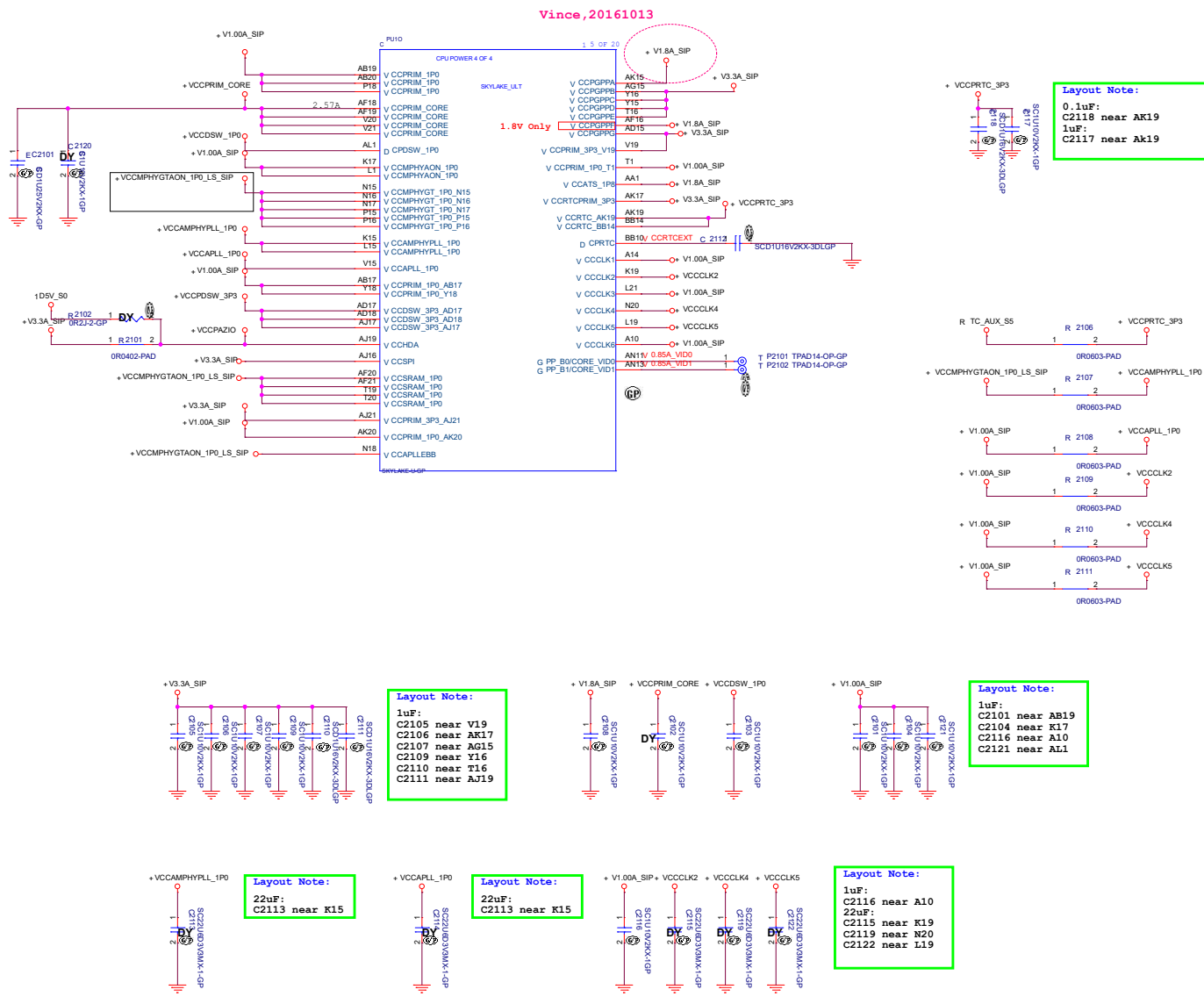
Vince,20170106



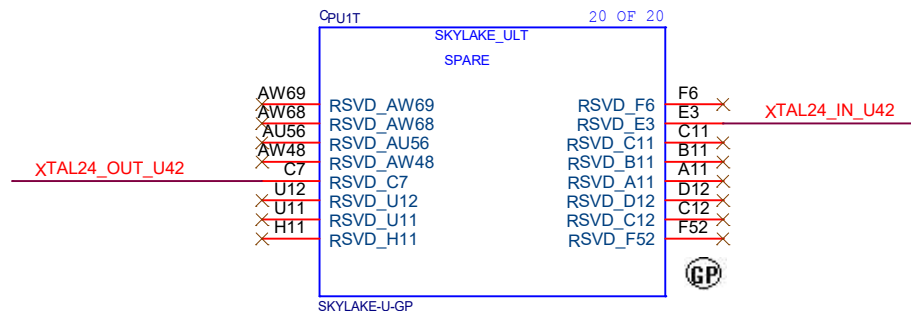
<Core Design>

SSID = PCH

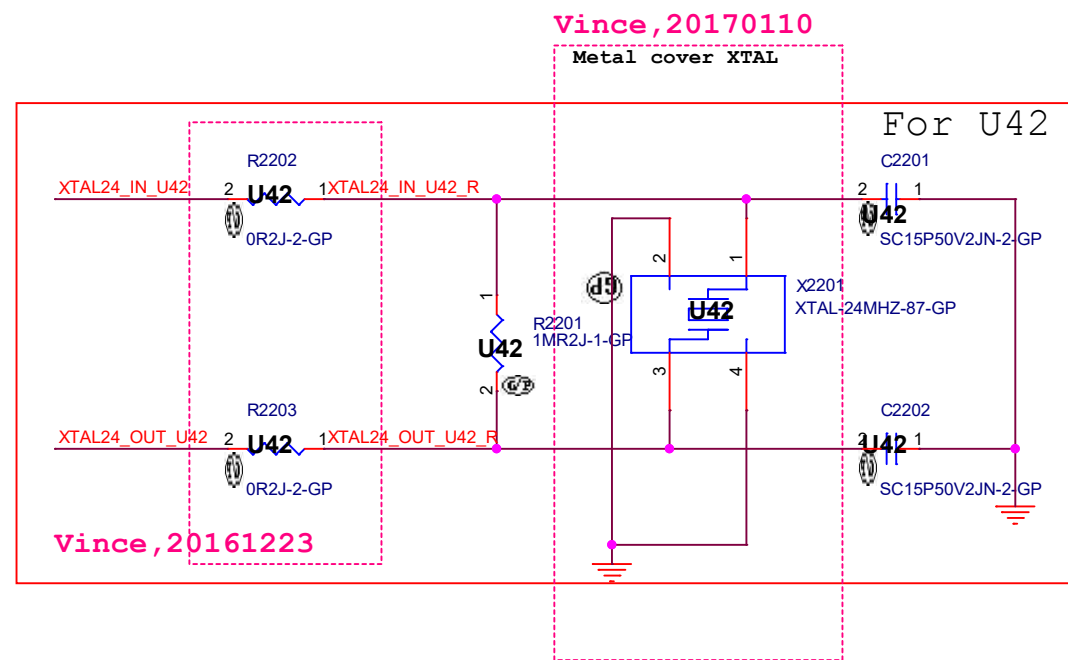




Main Func = PCH



Pin	Connection
#1,#3	X'tal
#2,#4	GND



<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU_(RSVD)

Size
A4

Document Number

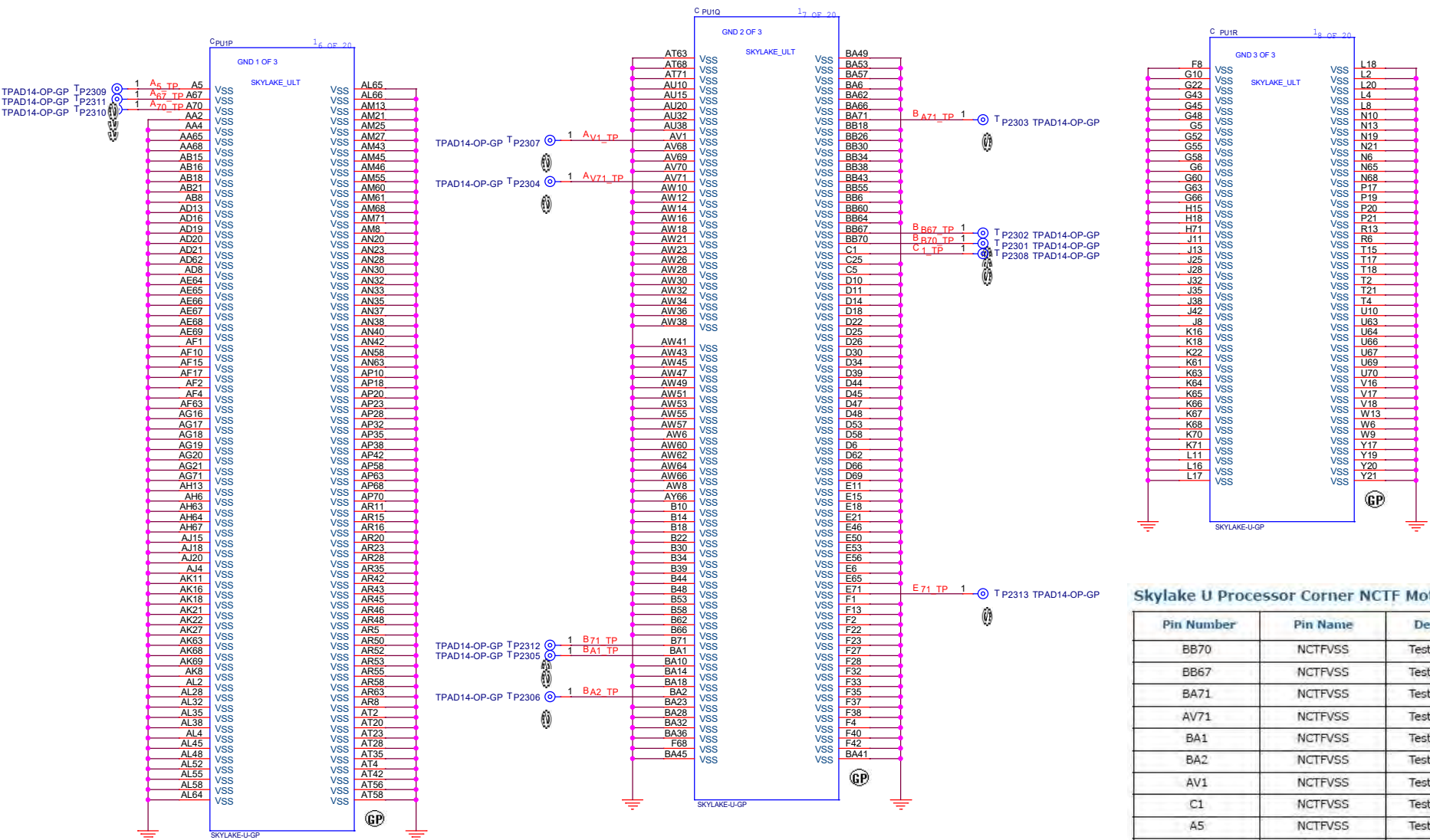
Starlord KBL-R

Rev
A 00

Date: Friday, December 08, 2017

Sheet 22 of 106

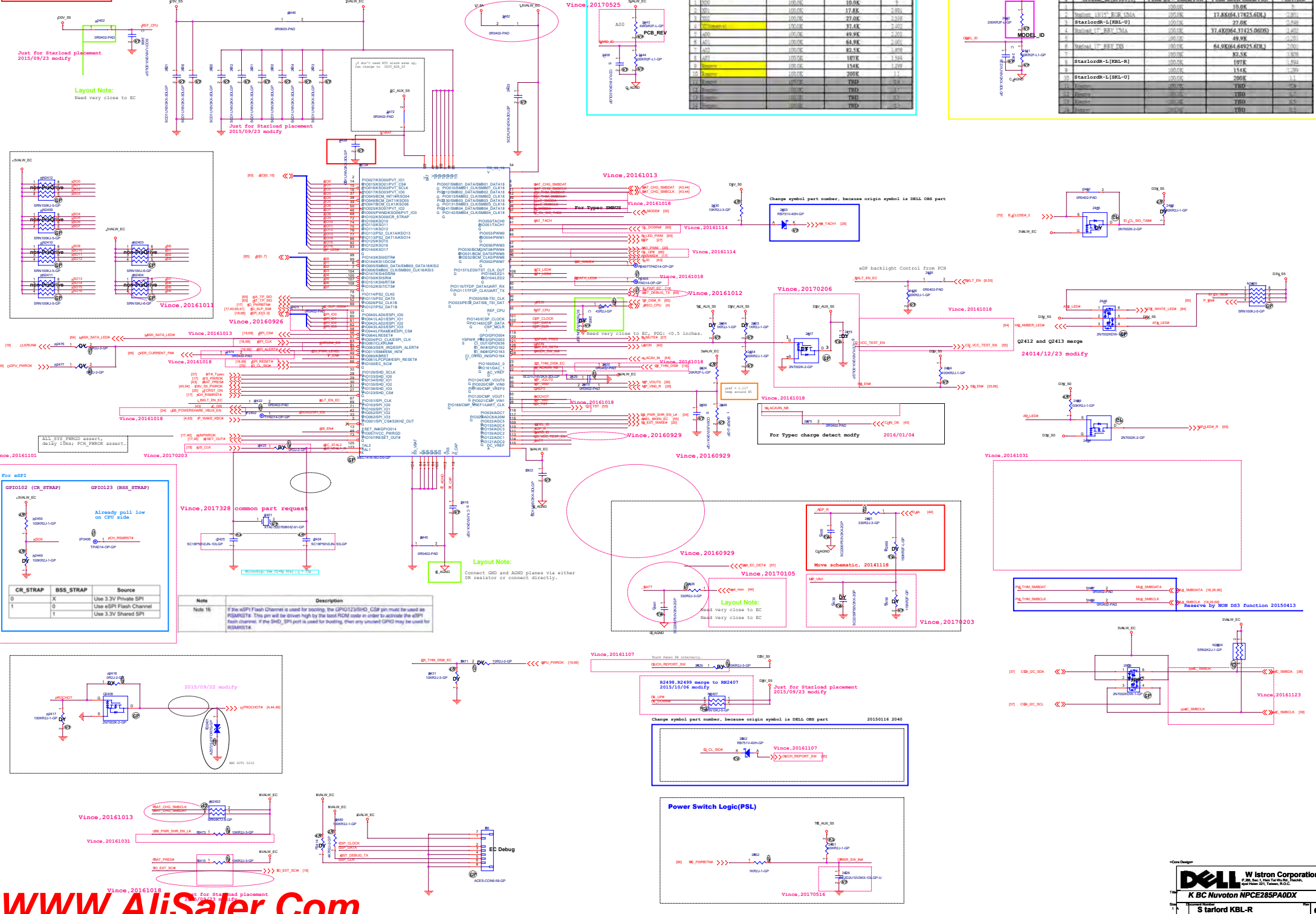
Main Func = PCH



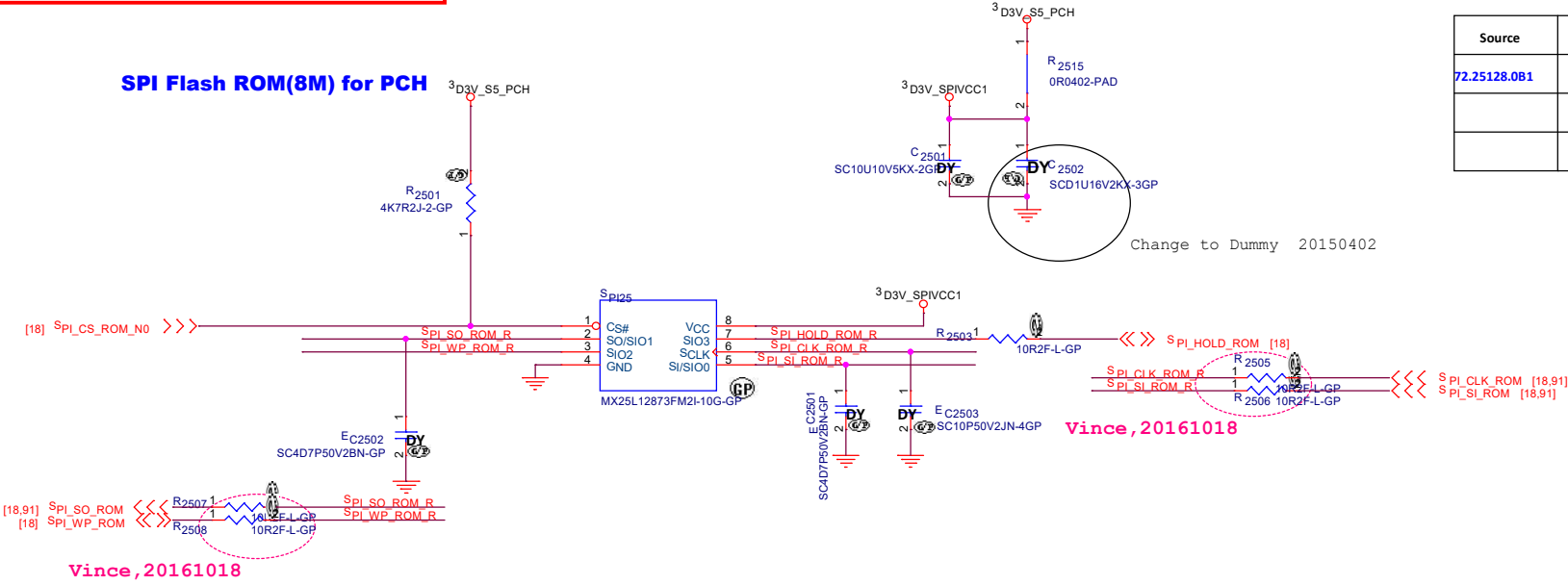
Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	Corner BB1
BA1	NCTFVSS	Test Point (TP)	
BA2	NCTFVSS	Test Point (TP)	Corner A1
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	Corner A71
A70	NCTFVSS	Test Point (TP)	
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

Main Func = KBC



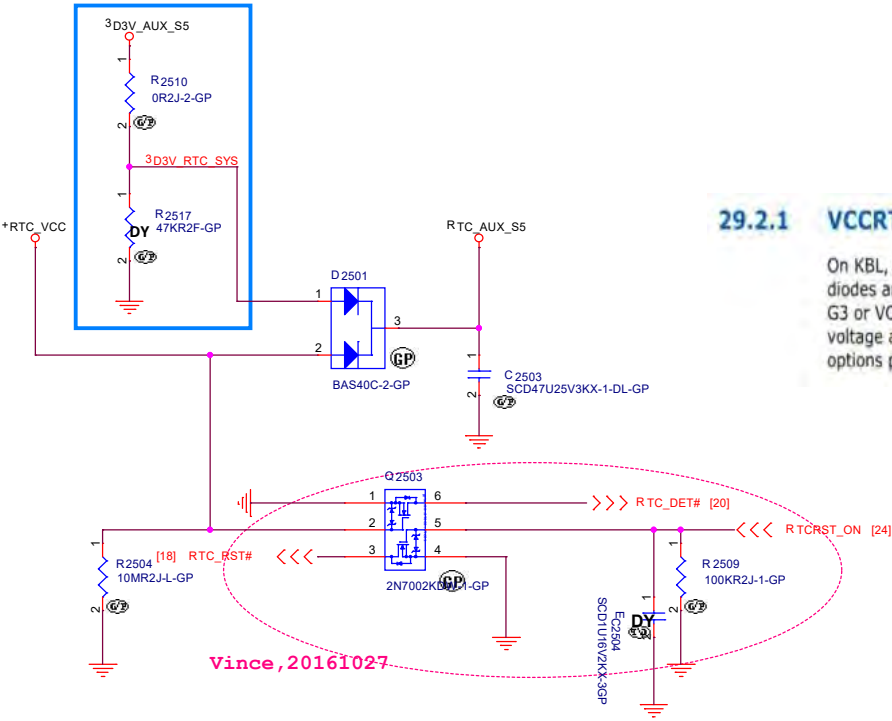
Main Func = SPI Flash



Source	QUAD/DUAL fast read	DUAL fast read	SFDP
72.25128.0B1	O	O	O
	O	O	O
	O	O	O

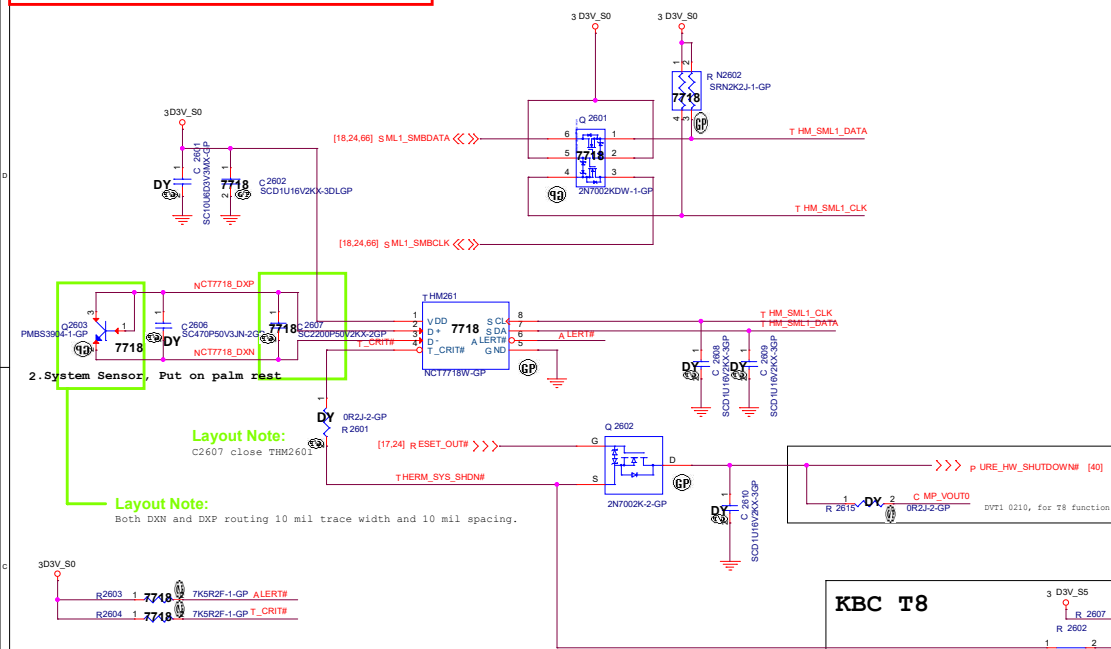
Delivery Voltage 3.19V
(when R2510 1K6 ohm)

Main Func = RTC

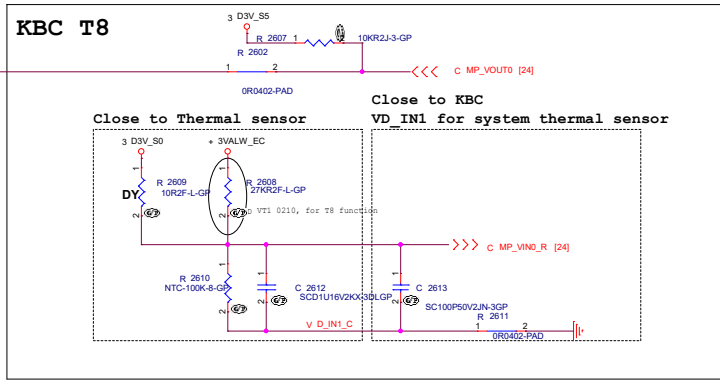


29.2.1 VCCRTC External Circuit

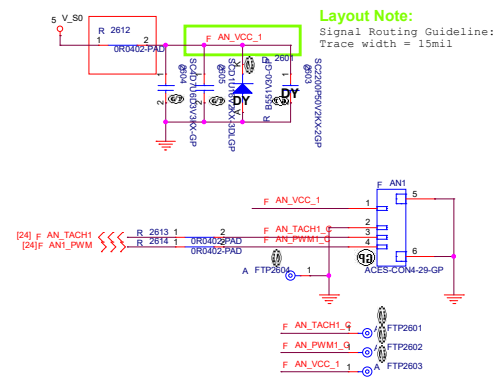
On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.



TEMPERATURE (°C)	T_CRIT#					
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ	
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



PWM FAN1

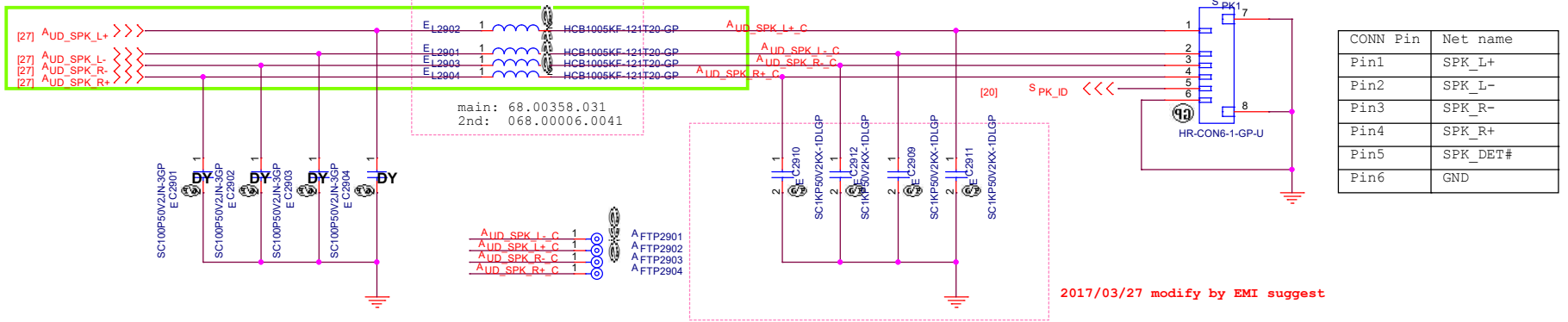


SSID = Audio

Layout Note:

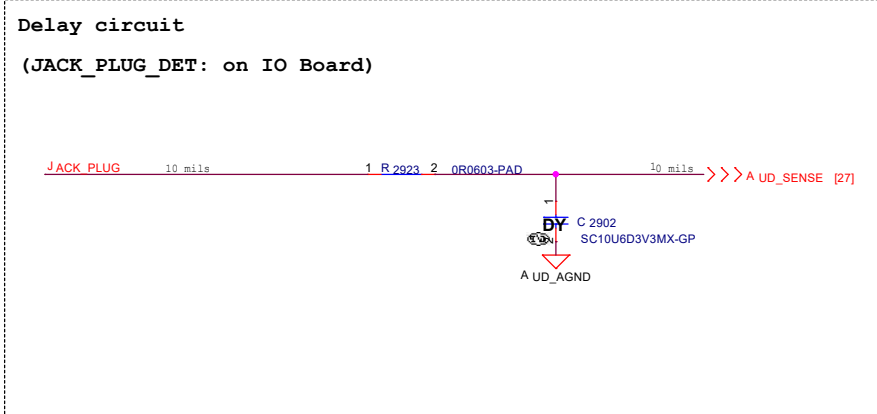
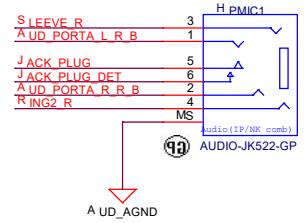
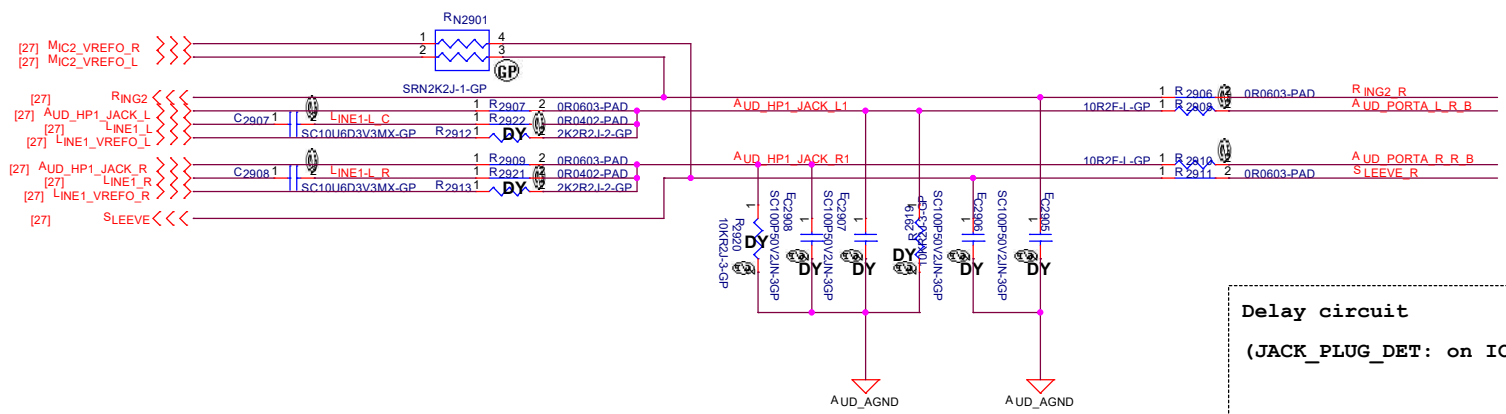
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

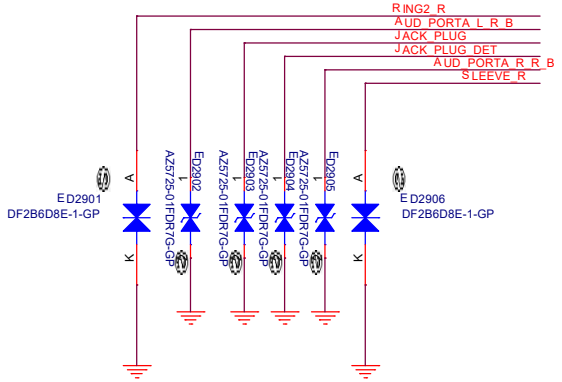


2017/03/27 modify by EMI suggest

Universal Jack (Moved to I/O Board)



CLOSS TO HPMIC1



Main Func = Audio

(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Starlord KBL-R		Rev A00
Date: Monday, August 28, 2017		Sheet 30 of 106	

(Blanking)


<Core Design>

		Wistron Corporation 2 - 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title LAN RTL8106			
Size A 3	Document Number Starford KBL-R		Rev A 00
Date Monday, August 28, 2017		Sheet 31	of 1
			108

SSID = LAN

(Blanking)

<Core Design>



Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

IT title

Size
A 3

Document Number
Starlord KBL-R


Rev
A00

Date: Monday, August 28, 2017Sheet 32 of 106

Main Func = Card Reader

(Blanking)

<Core Design>



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Taippei Hsien 221, Taiwan, R.O.C.

Title

Card Reader-RTS5170

Size

A 3

Document Number

S tarlord KBL-R

Rev

A 00

Date

Monday, August 28, 2017

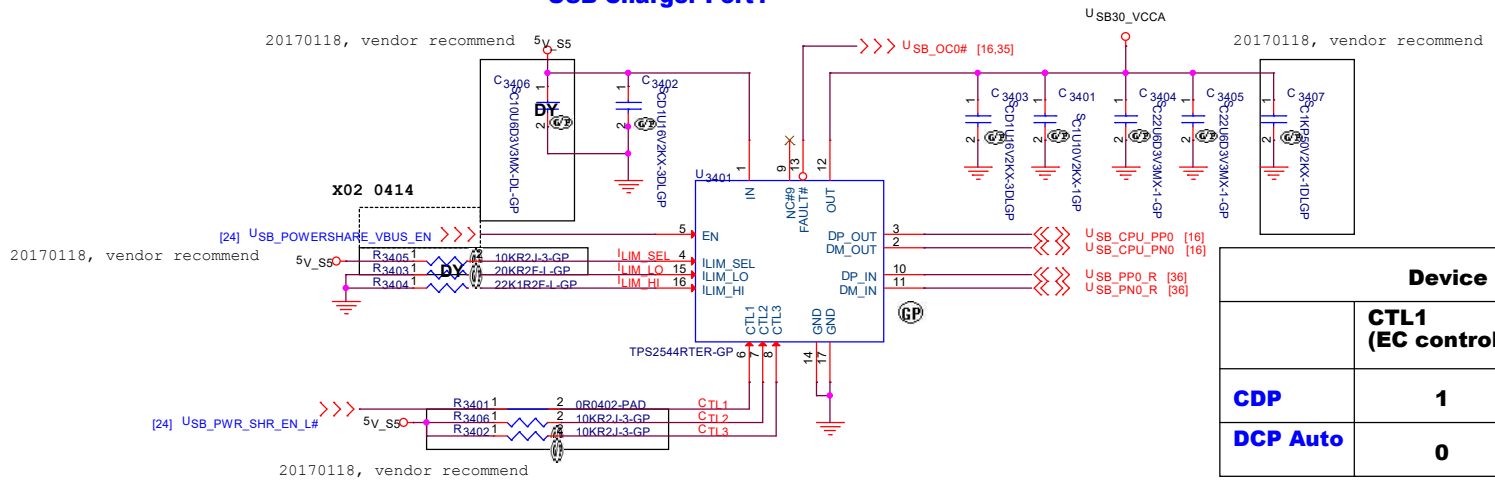
Sheet

S3

o 1

108

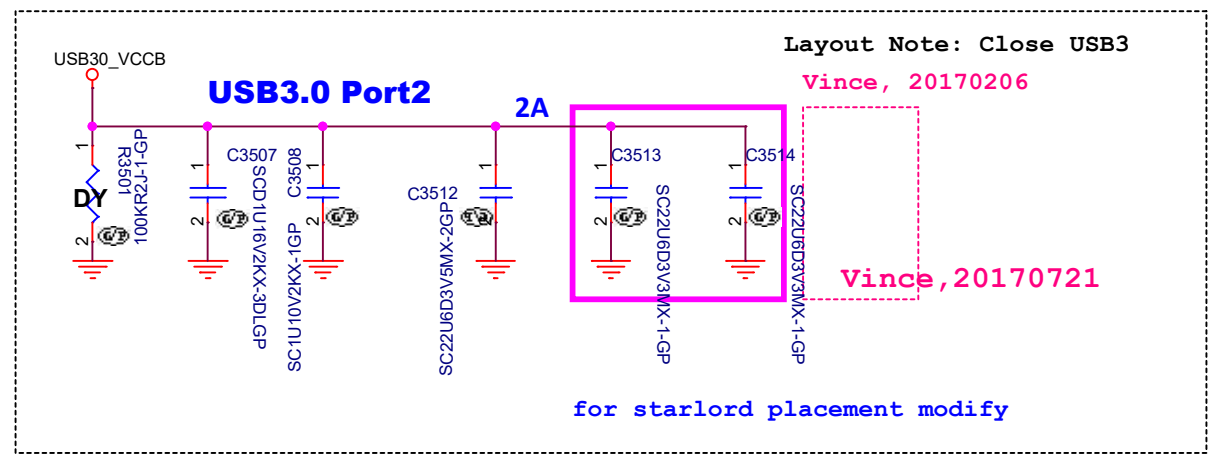
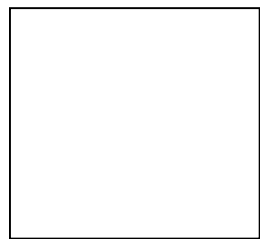
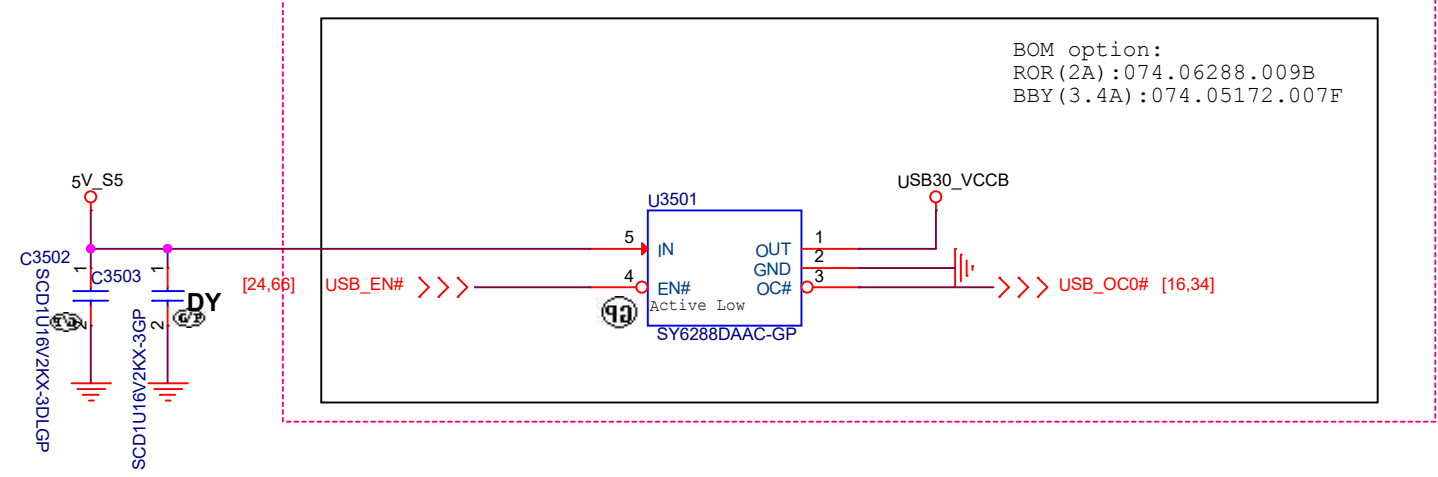
USB Charger Port1




Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

Main Func = USB3.0 Port1

Vince, 20170206



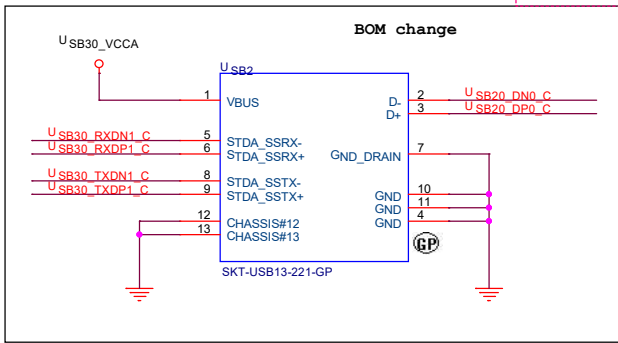
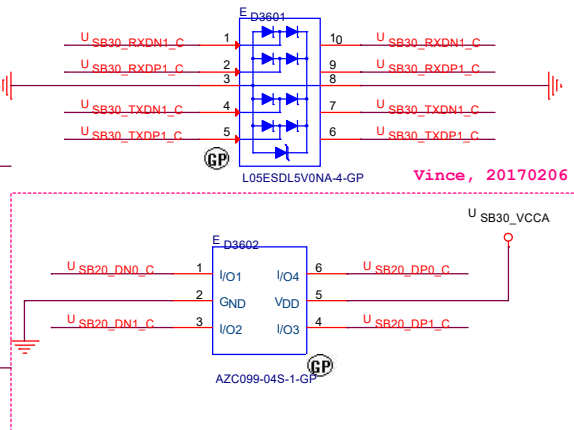
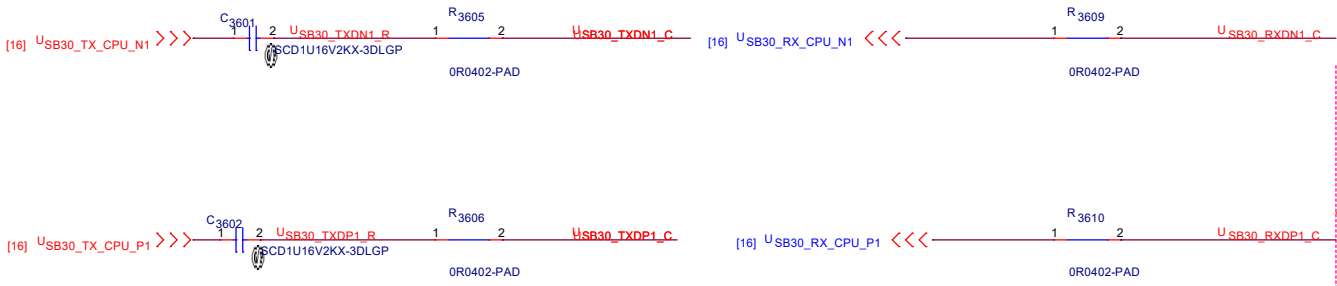
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title USB switch			
Size	Document Number Starlord KBL-R		Rev A 00
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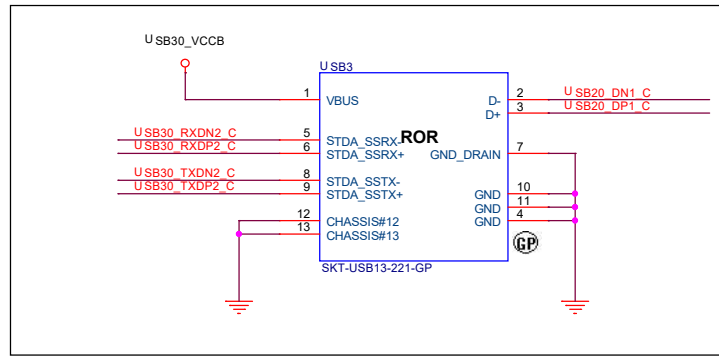
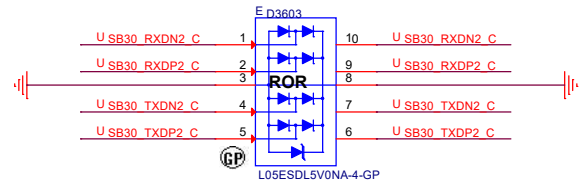
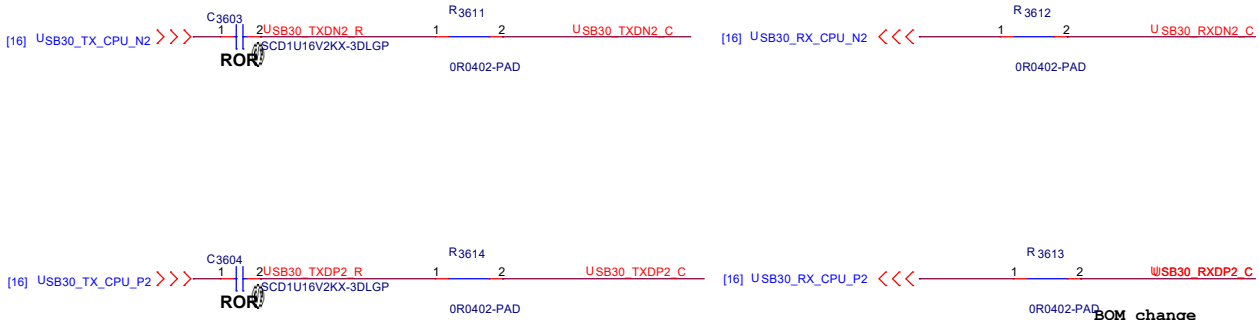
SSD = USB3.0 Port1

USB2.0 Port2 and USB2.0 Port3 are on IOBD

USB3.0 Port1



USB3.0 Port2



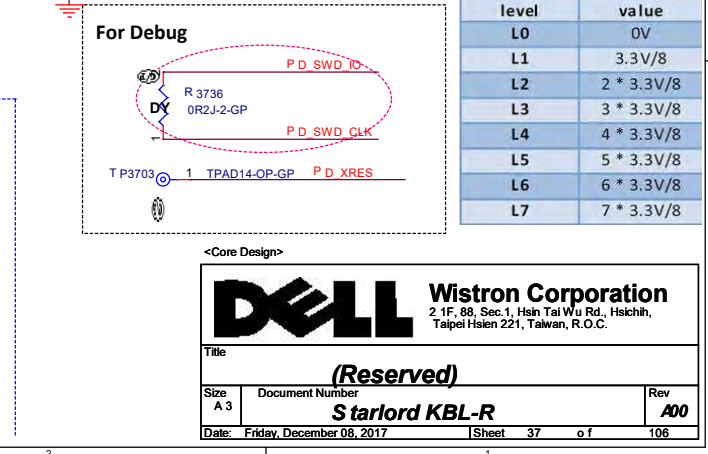
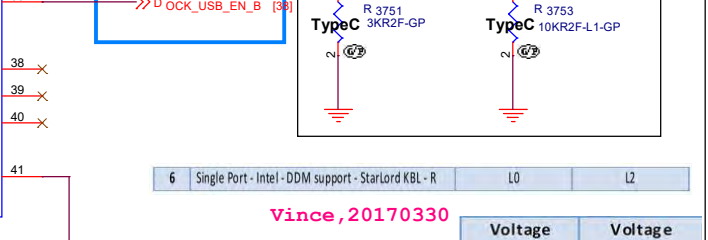
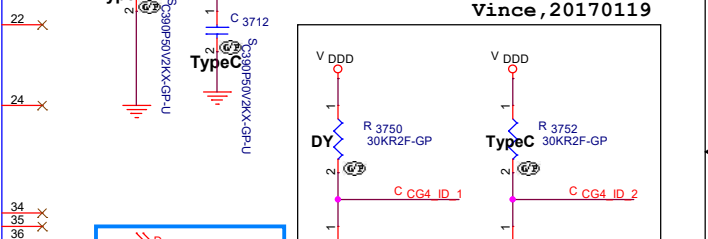
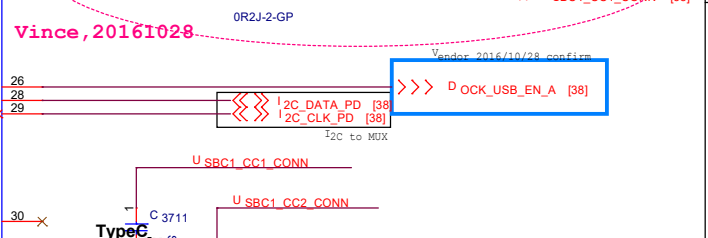
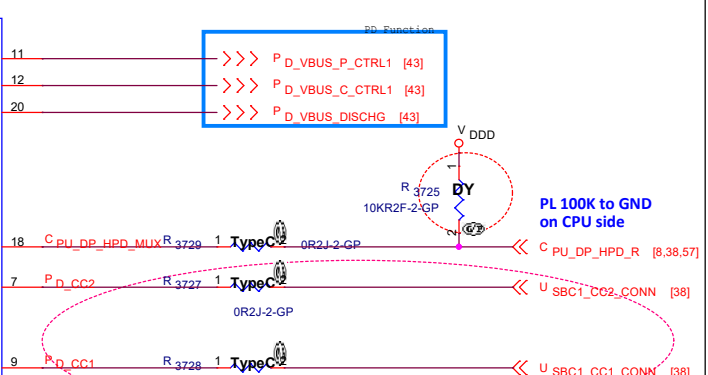
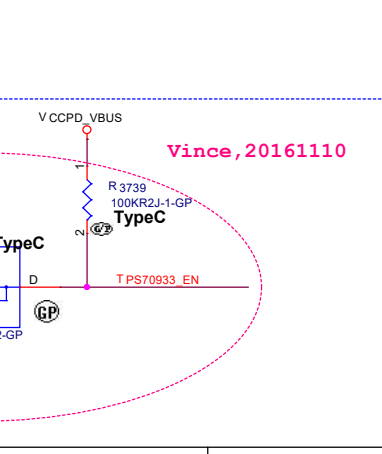
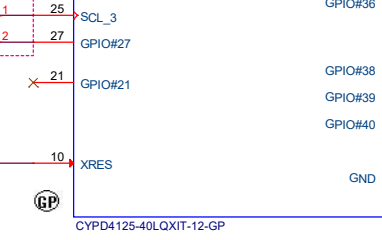
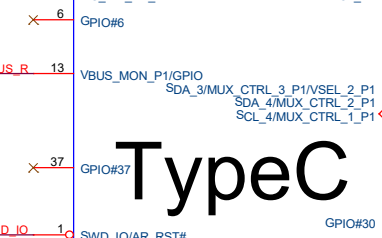
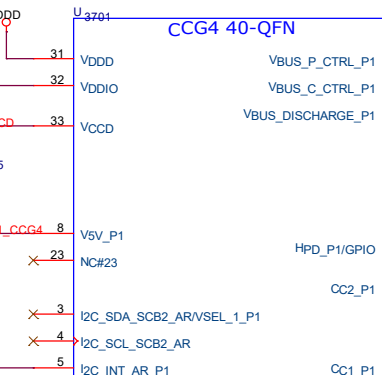
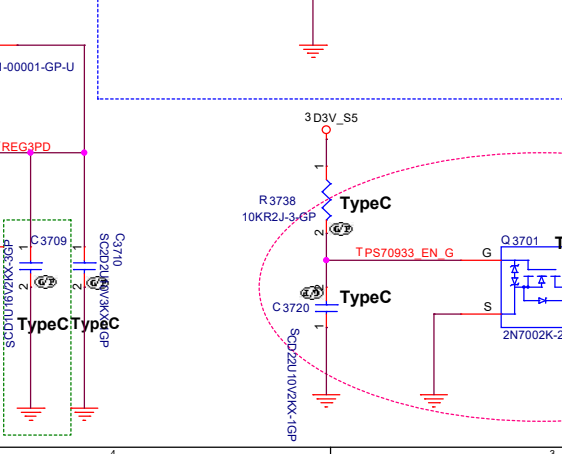
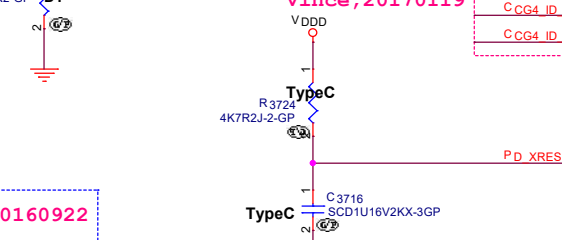
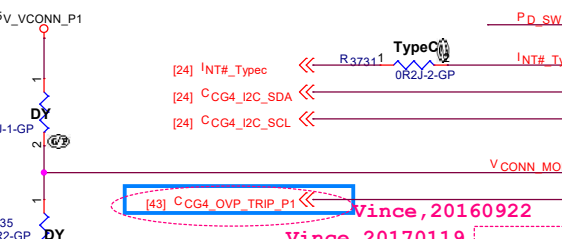
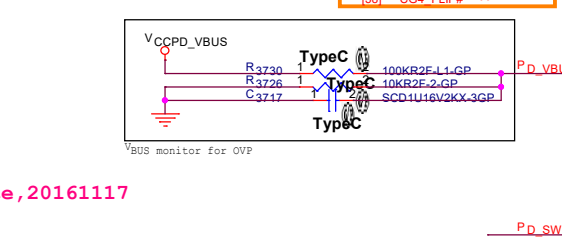
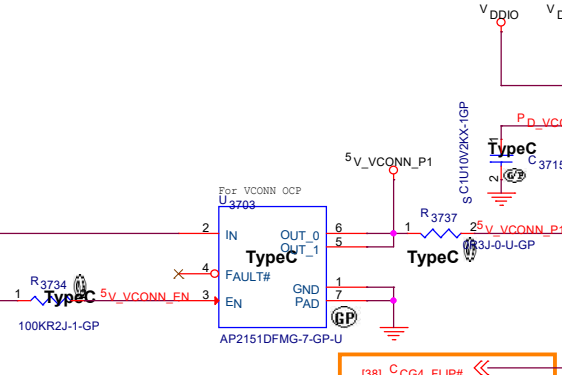
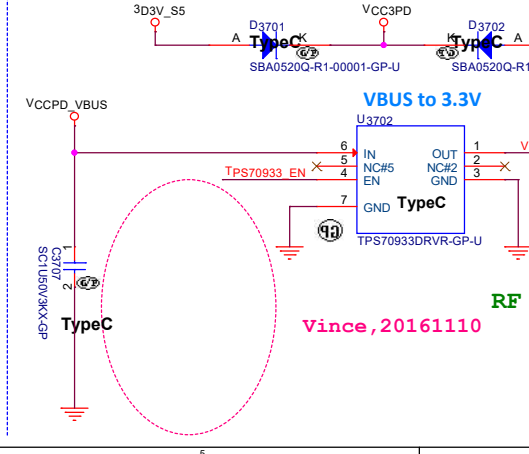
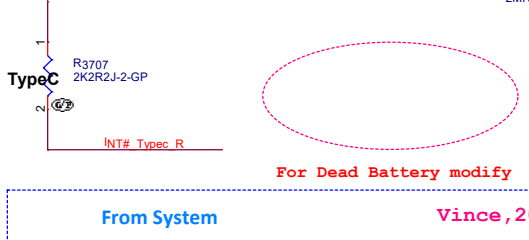
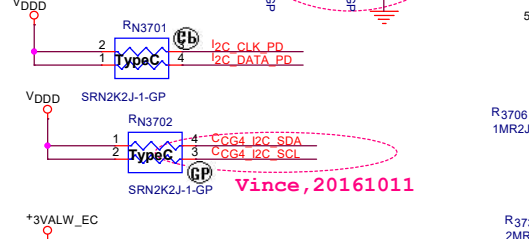
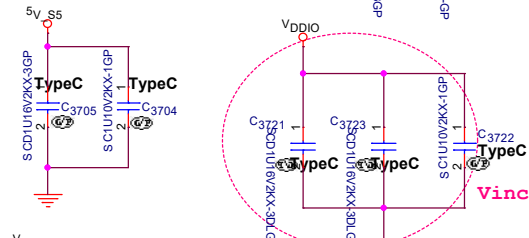
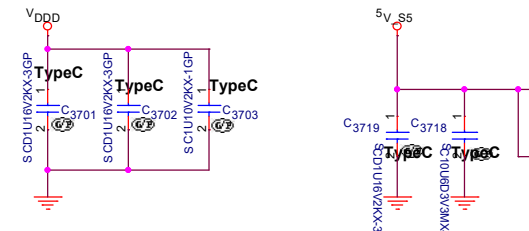
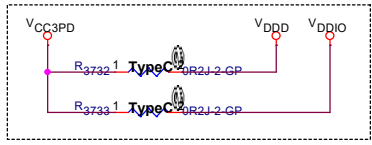
<Core Design>

DELL Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB30**

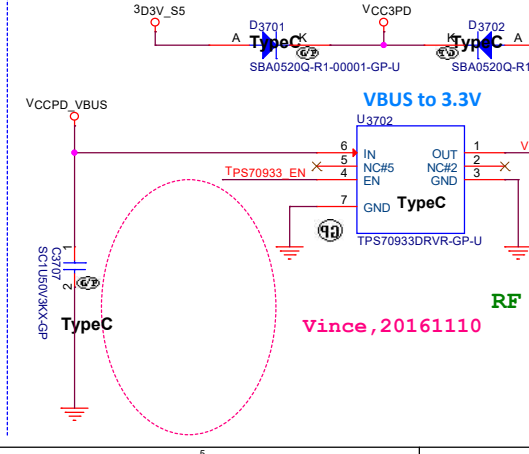
Size: A3 Document Number: **Sstarlord KBL-R** Rev: **A00**

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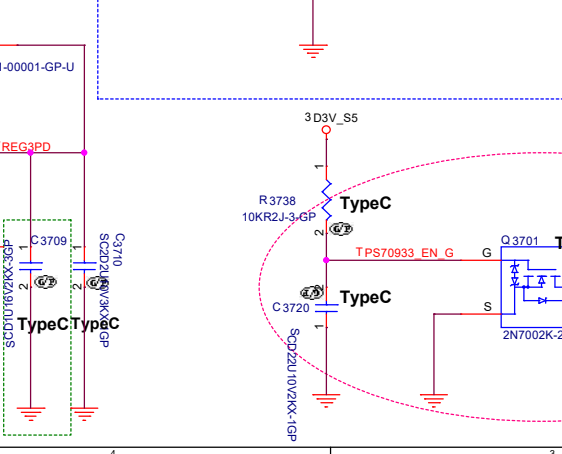


TypeC

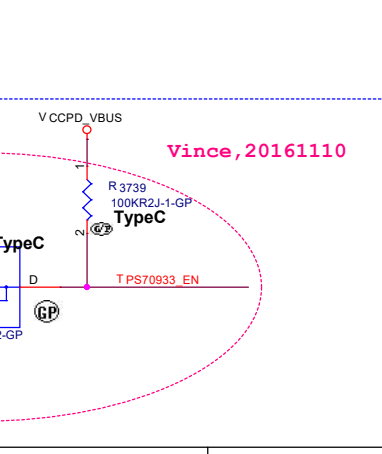
For Dead Battery modify



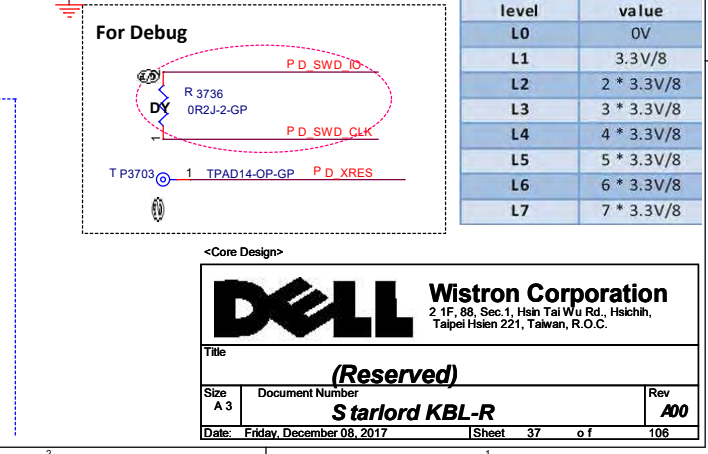
Vince, 20161117



Vince, 20161028

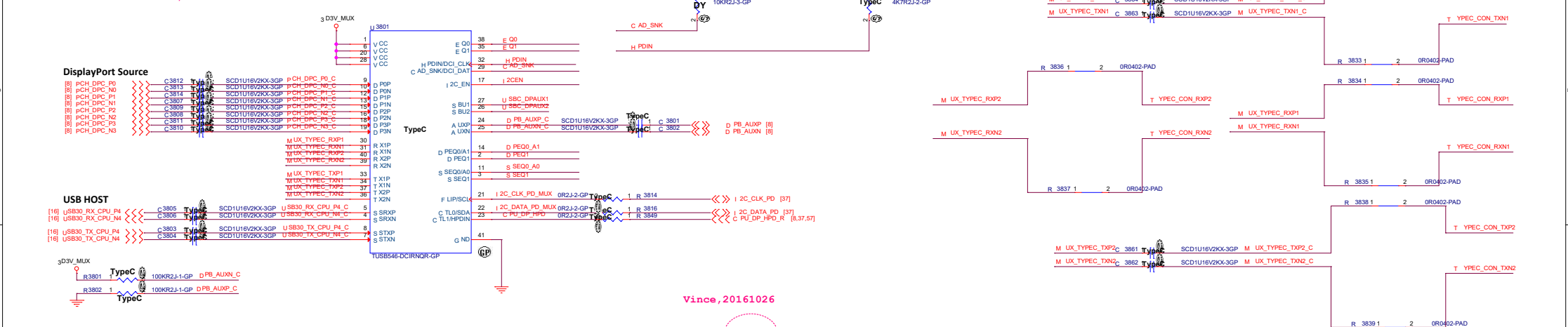


Vince, 20161028

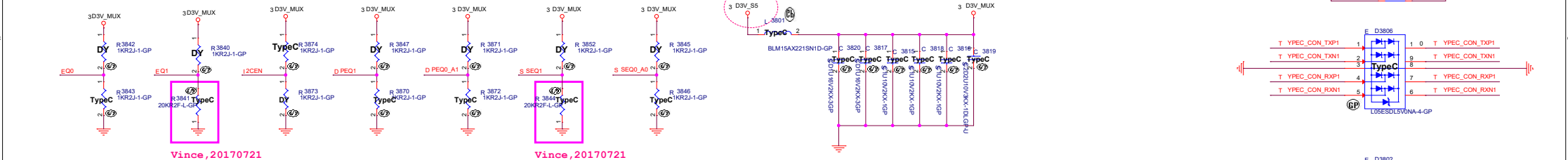


Main Func = TYPEC MUX

Vince, 20161012



Vince, 20161026

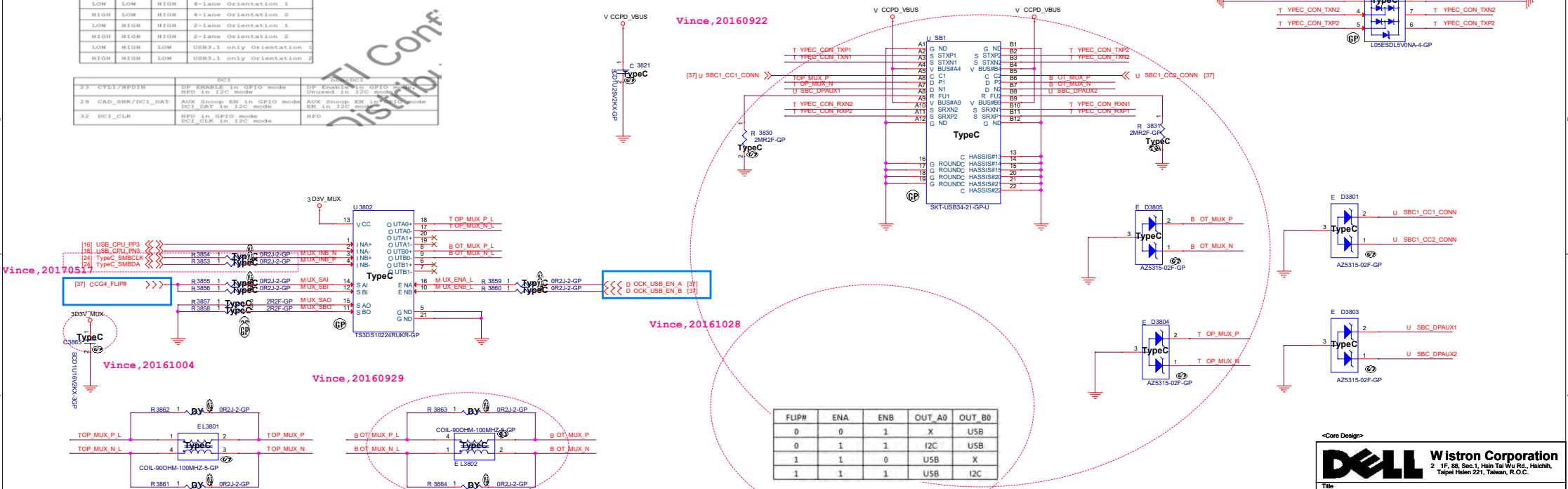


Vince, 20170721

Vince, 20170721

CELL POL	CELL ANSEL	CELL EN	Mux Operation
X	LOW	LOW	POWER DOWN
LOW	LOW	HIGH	4-lane Orientation 1
HIGH	LOW	HIGH	4-lane Orientation 2
LOW	HIGH	HIGH	2-lane Orientation 1
HIGH	HIGH	HIGH	2-lane Orientation 2
LOW	HIGH	LOW	USB3.1 only Orientation 1
HIGH	HIGH	LOW	USB3.1 only Orientation 2

	DCI	non-DCI
23 CTL1/RPDI	DF ENABLE in GPIO mode RPDI in I2C mode	DF Enable in GPIO mode, Unused in I2C mode
29 CAD_ENR/DCI_DAT	AUX Snoop En in GPIO mode DCI_DAT in I2C mode	AUX Snoop En in GPIO mode En in I2C mode
32 DCI_CLK	RPDI in GPIO mode DCI_CLK in I2C mode	RPDI



Vince,20160922

Vince, 20161028

FLIP#	ENA	ENB	OUT_A0	OUT_B0
0	0	1	X	USB
0	1	1	I2C	USB
1	1	0	USB	X
1	1	1	USB	I2C

<Core Design>


DELL **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
(Reserved)			
Size A 2	Document Number S tarlord KBL-R	Rev A 0	
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WWW.AliSaler.Com

Main Func = USB3.0 Port1

<Core Design>

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Title (Reserved)					
Size A 3	Document Number S tarford KBL-R				Rev A 00
Date Monday, August 28, 2017		Sheet 39		of 1 108	

Power Good

[52]1 DOV_S5_PWRGD >>> R 4029 1 2 0R402-PAD

[24,54]1 D8V_S5_PWROK >>> R 4030 1 2 0R403-PAD

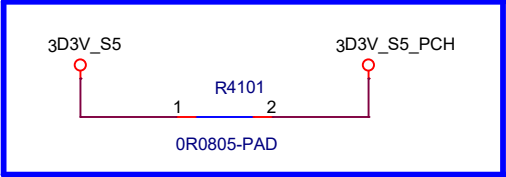
[17,45,52,54]3 V_5V_POK >>> R 4033 1 2 0R403-PAD

NON DS3: PH 3V_5V_POK to 3D3V_AUX_S5 at page17

change common part PN:074.05027.0093, 20170302



Main Func = Power Plane & Sequence




Reserve by NON DS3 function 20150413

Vince,20161031


DS3

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Connected_Standby(1/2)+DS3		
Size A4	Document Number Starlord KBL-R	Rev A 00
Date: Friday, December 08, 2017		Sheet 41 of 106

Main Func = DIMM1
Main Func = DIMM2

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Connected_Standby(2/2)

Size

A 3

Document Number

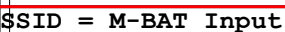
Starlord KBL-R

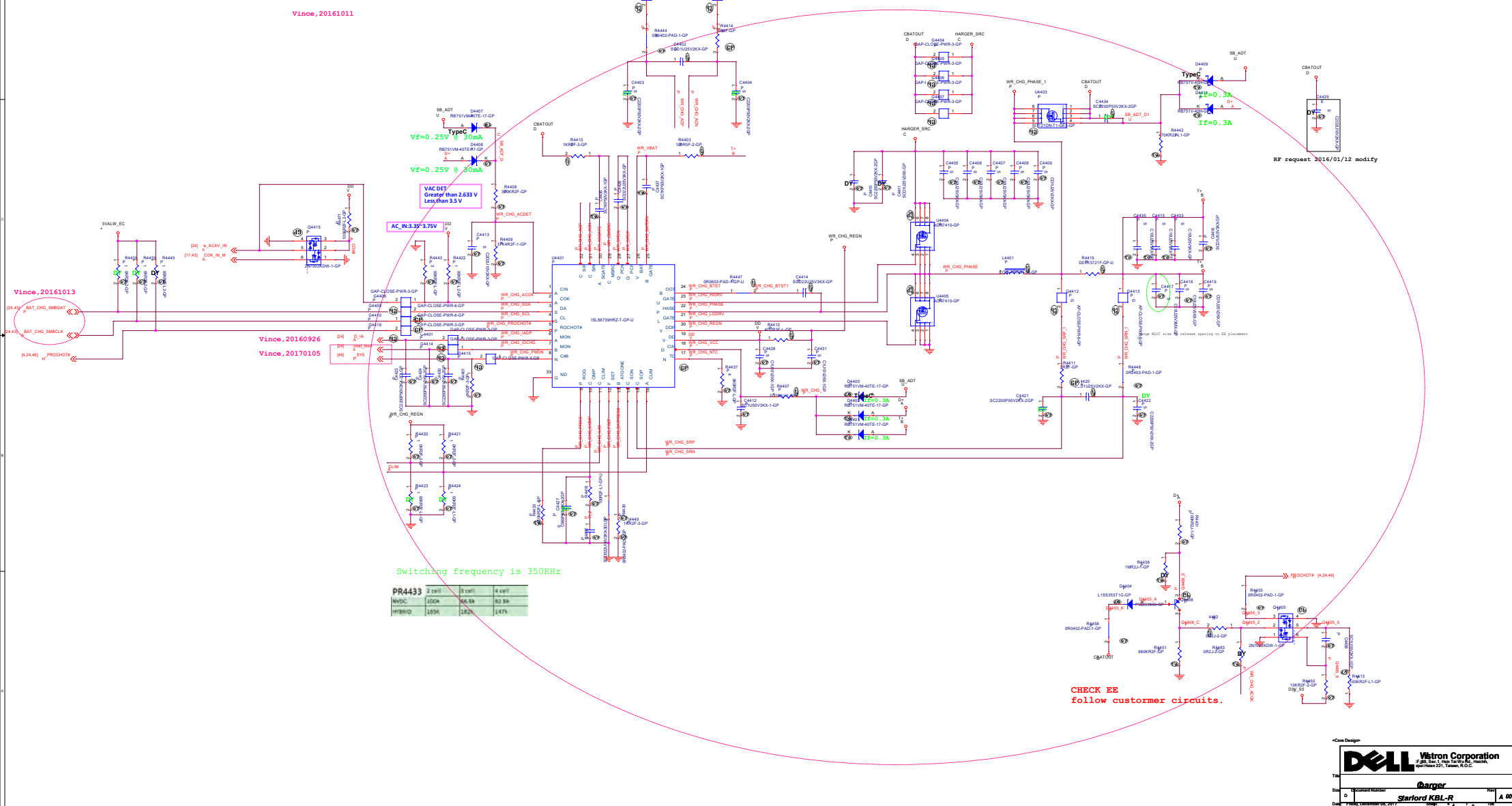
Rev

A 00

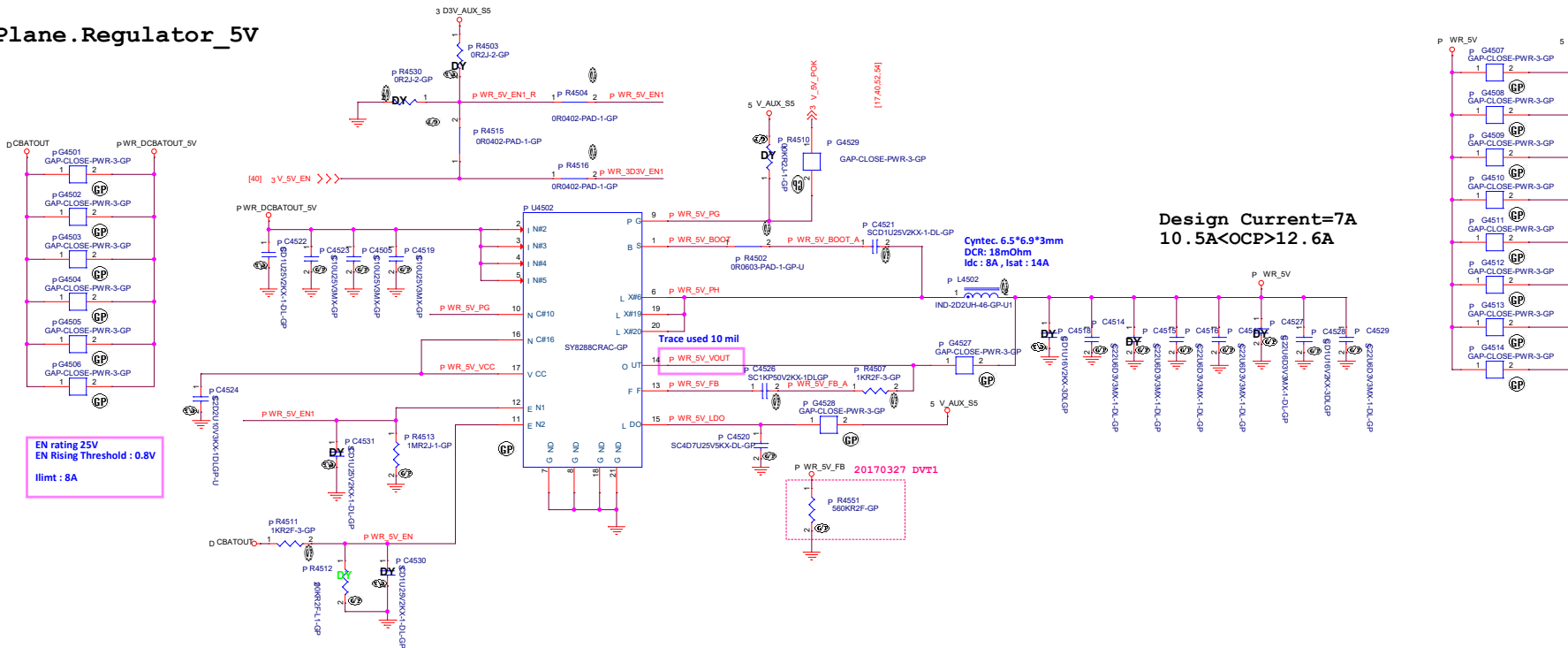
Date: Monday, August 28, 2017Sheet 42 of 106

Pin Definition: TBD

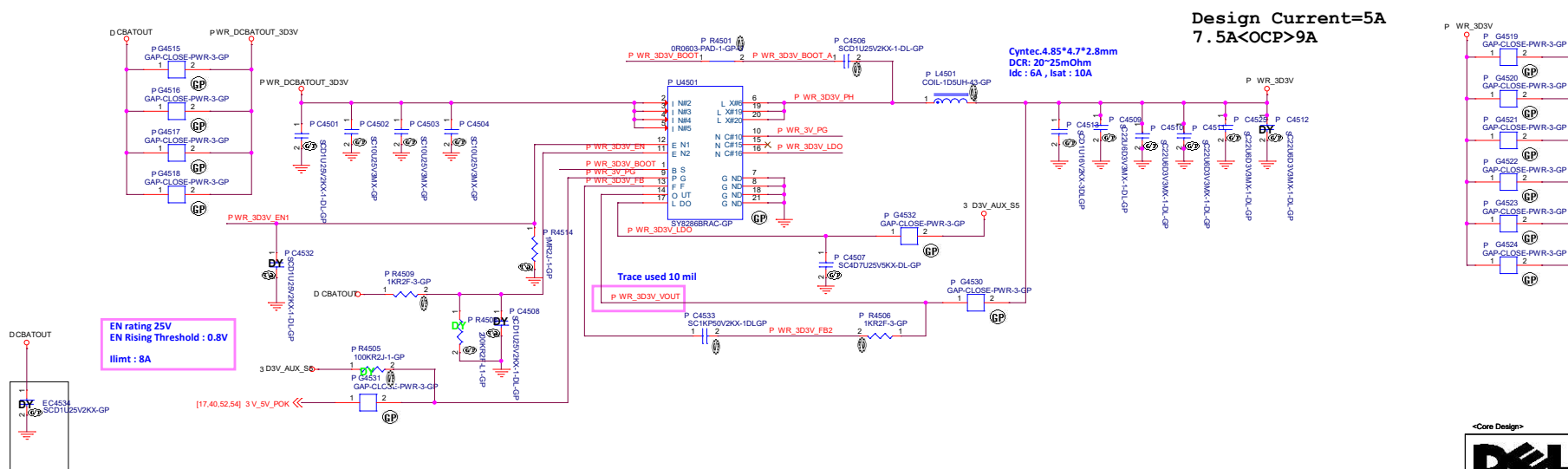


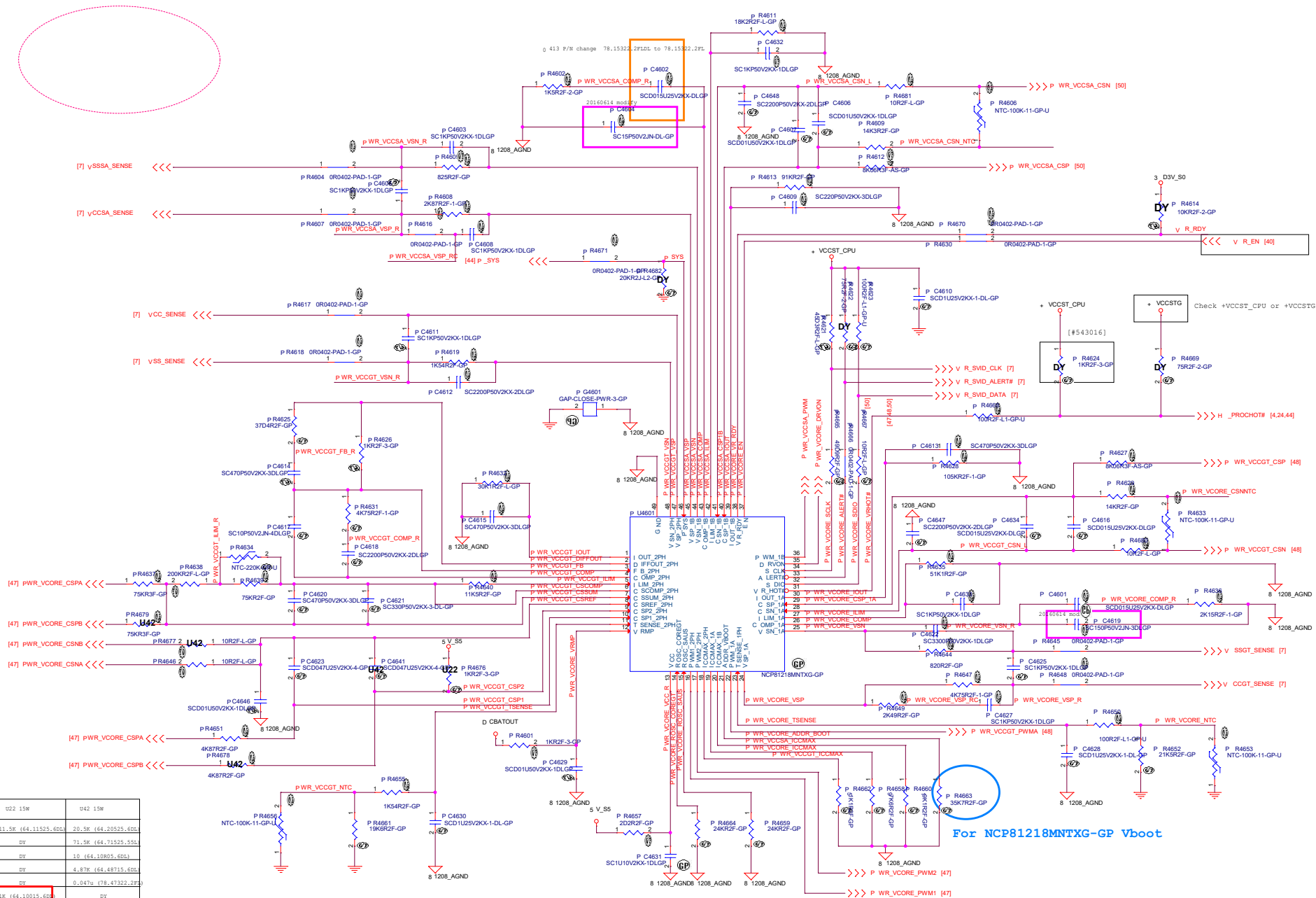


SSID = PWR.Plane.Regulator_5V



SSID = PWR.Plane.Regulator_3D3V





	022 15W	042 15W
PR4640	11.5K (64.11525, 60S)	20.5K (64.20525, 60S)
PR4679	DY	71.5K (64.71525, 55S)
PR4677	DY	1.0 (64.10805, 60S)
PR4678	DY	4.97K (64.48715, 60S)
PC4644	DY	0.047u (18.47322, 28F)
PR4676	1K (64.10015, 60S)	DY
PR4662	11.1K (64.11125, 60S)	100K (64.10035, 60S)
PR4659	97.6K (64.97625, 60S)	97.6K (64.97625, 60S)
PR4635	51.1K (64.51125, 60S)	51.1K (64.51125, 60S)
PR4628	105K (64.10535, 60S)	105K (64.10535, 60S)
PR4632	30.1K (64.30125, 60S)	26.1K (64.26125, 60S)

20170208

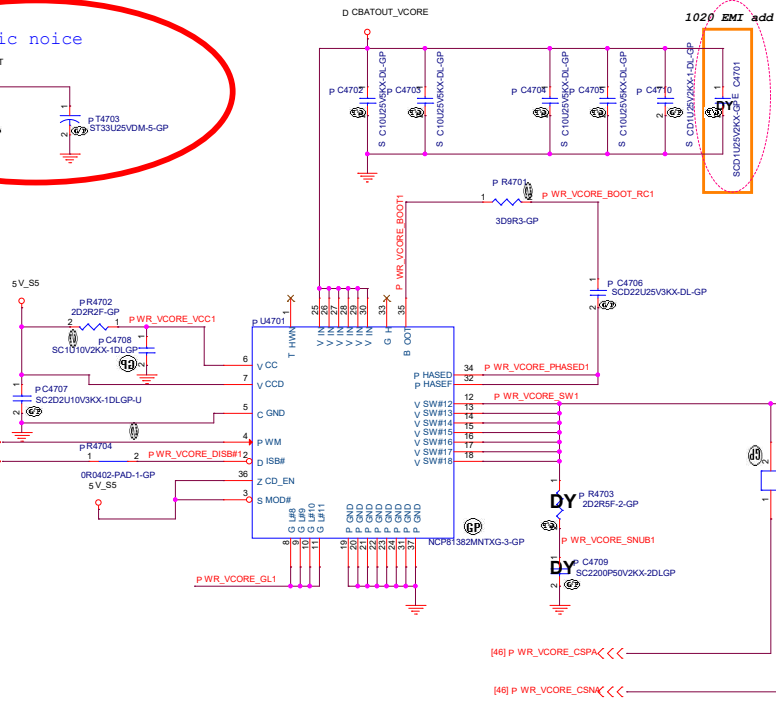
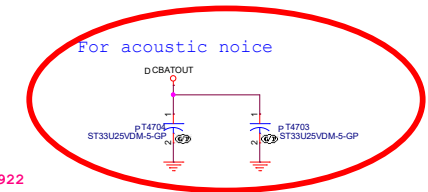
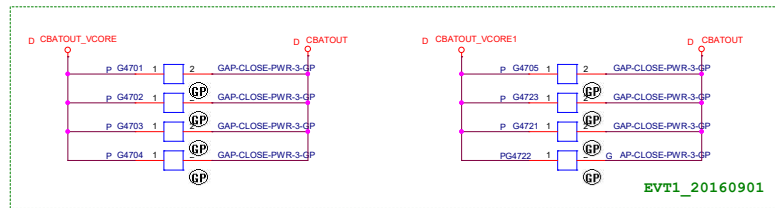
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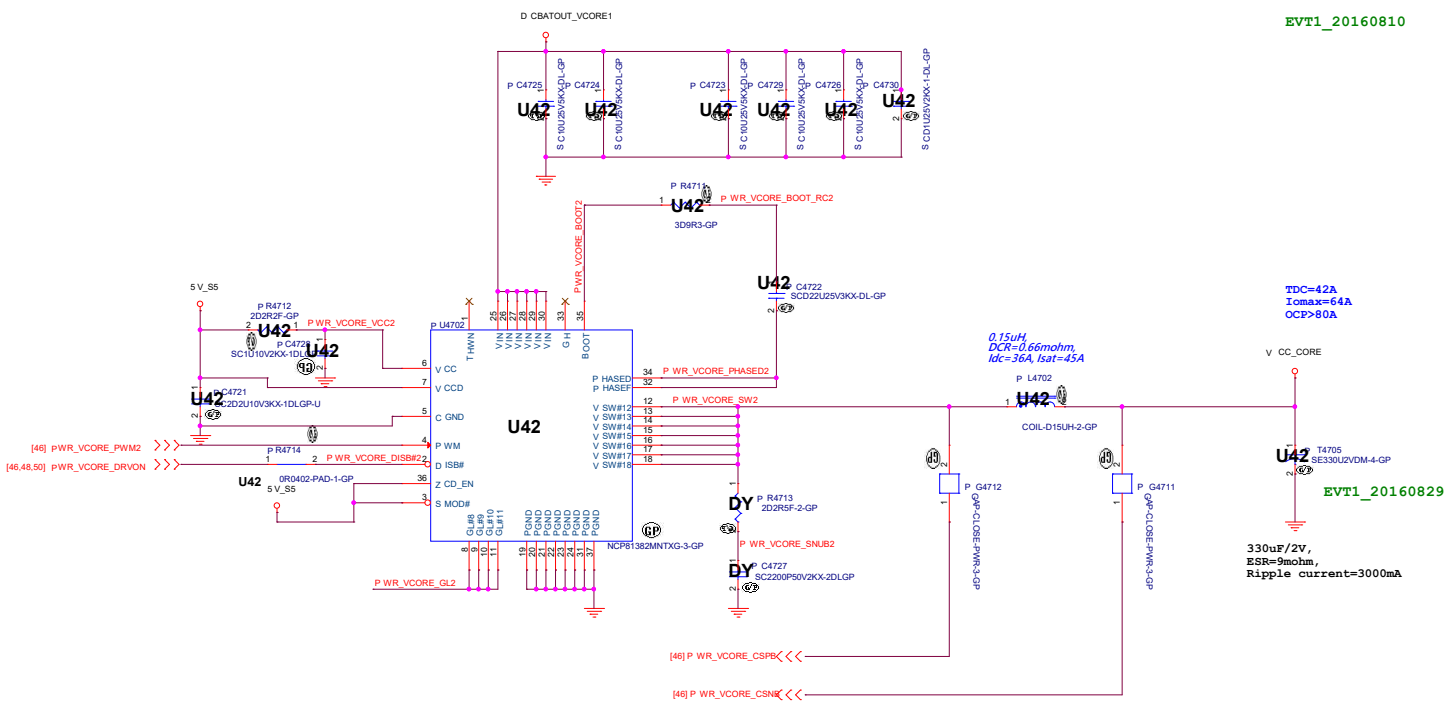
Vince,20161020

For acoustic noise

Vince,20160922



EVT1_20160810



TDC=42A
Iomax=64A
OCP>80A

EVT1_20160829

<Core Design>

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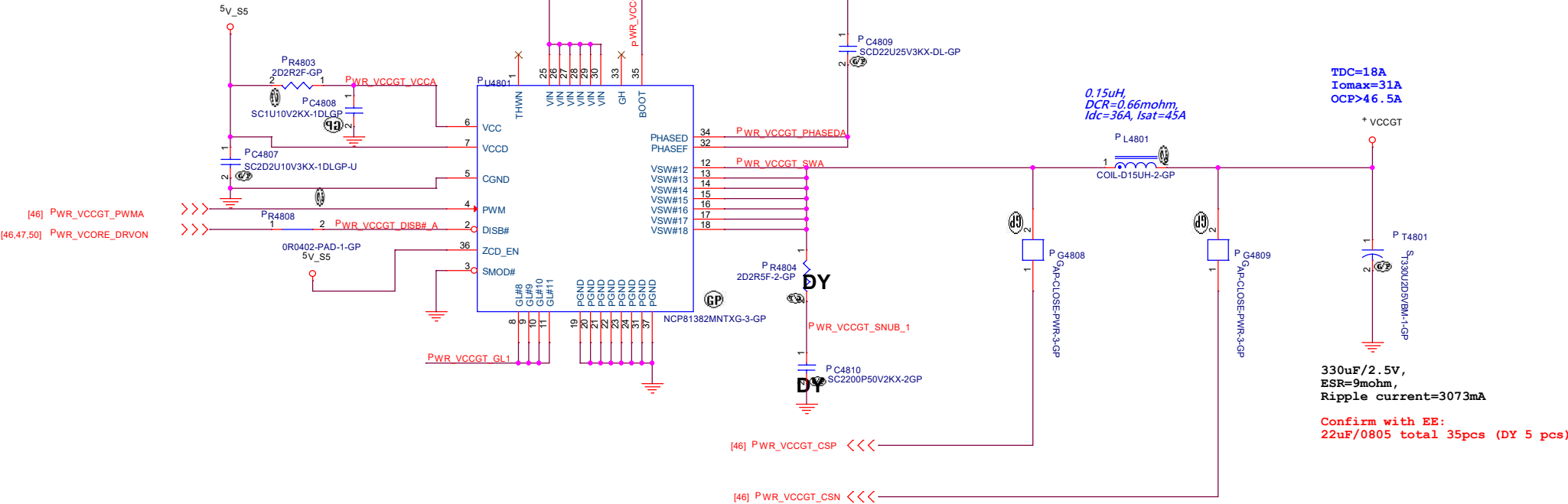
Vince,20160929

Vince,20160922

Vince,20160929

Vince,20161020

1020 EMI add



Main Func = CPU_CORE

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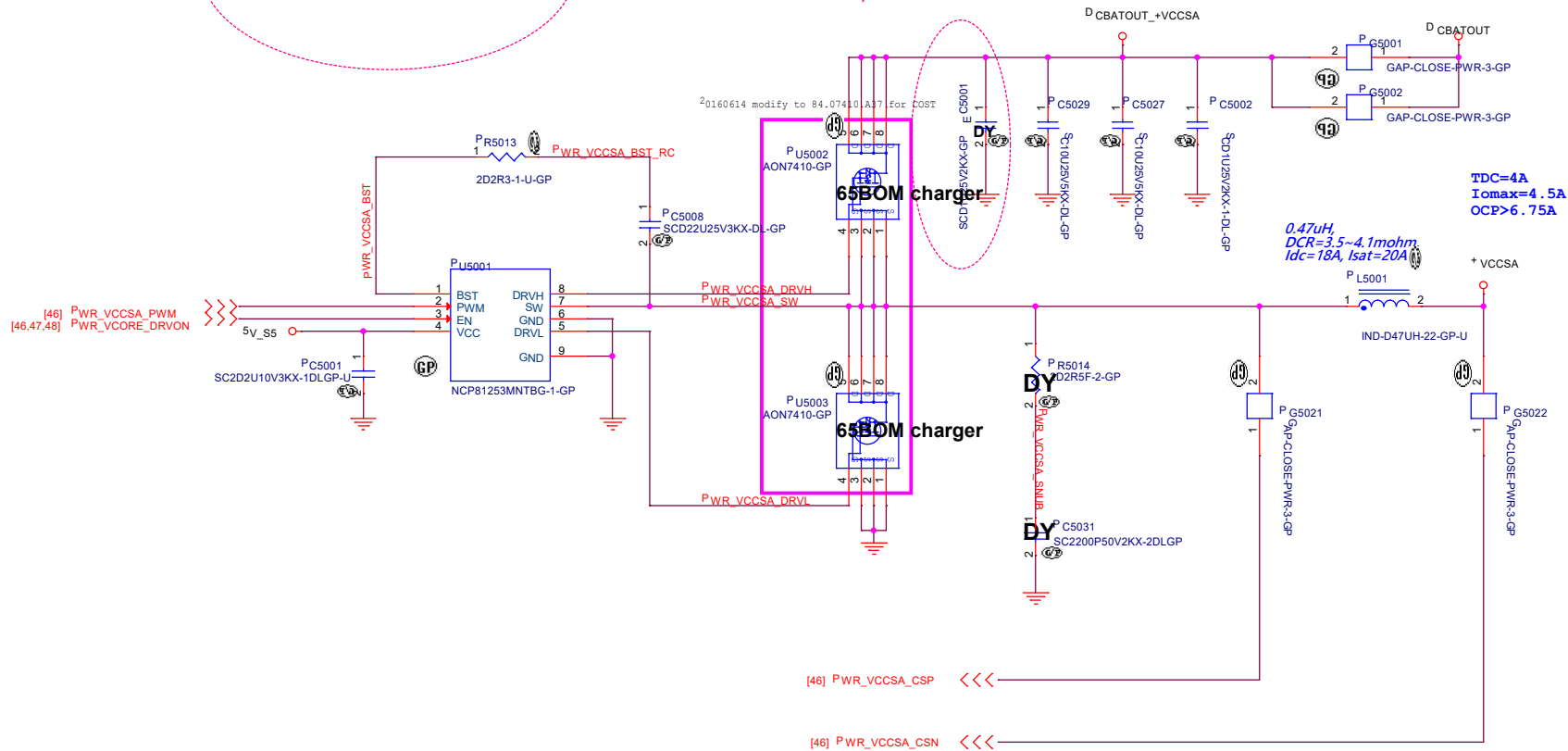
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title NCP81210MN_CPU_VCCGTUS		
Size A4	Document Number Starlord KBL-R	Rev A 00
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Main Func = CPU_CORE

Vince,20160922

Vince,20161020



Confirm with EE:
22uF/0805 total 20pcs (DY 5 pcs)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title **NCP81253MN_CPU_VCCSA**

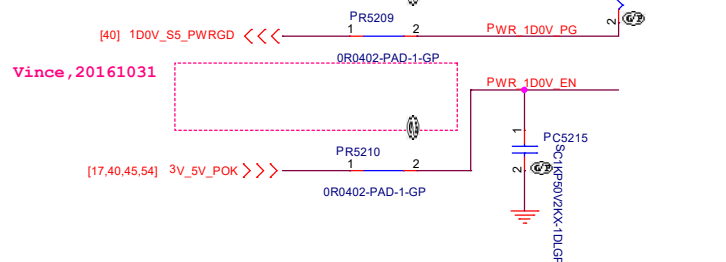
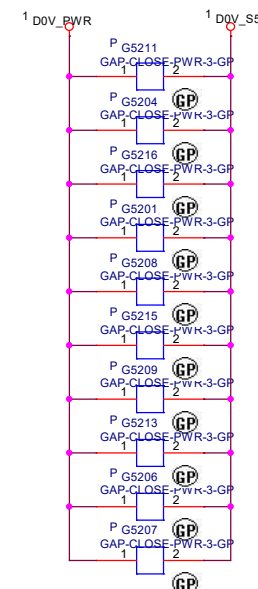
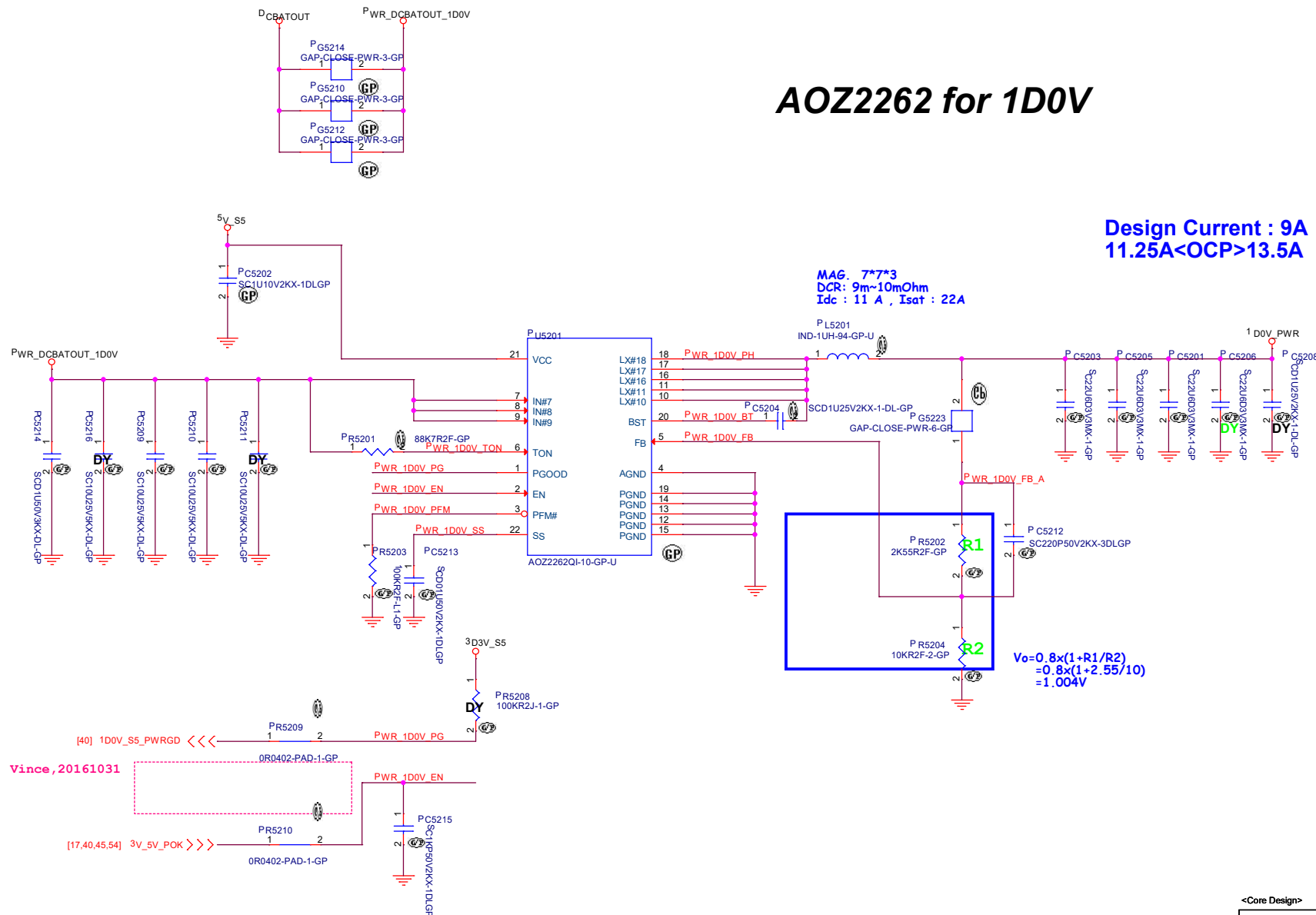
Size A 3	Document Number Starlord KBL-R	Rev A00
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SSID = PWR.Plane.Regulator_1D0V

AOZ2262 for 1D0V

Design Current : 9A
11.25A<OCP>13.5A



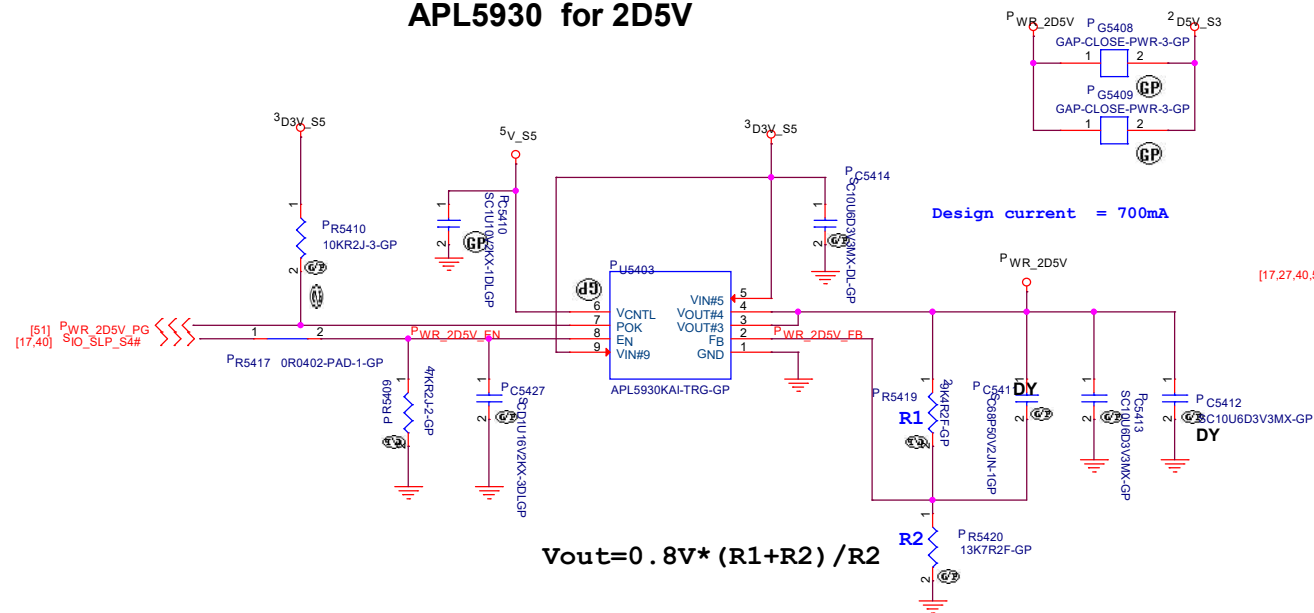
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4					
3					
2					
1					

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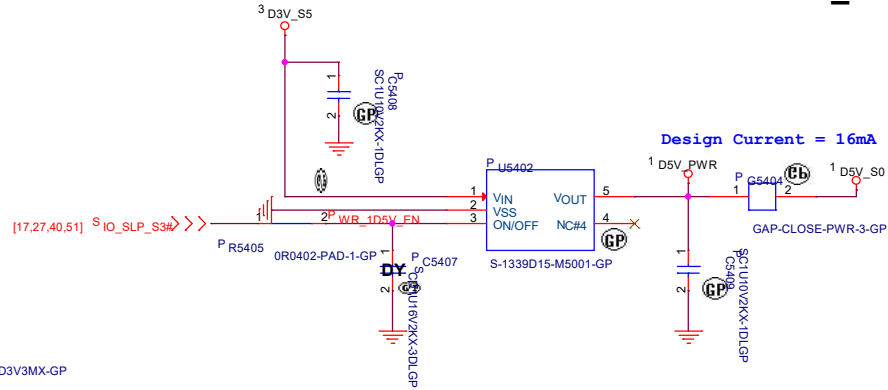
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Title (Reserved)			
Size A 3	Document Number Starlord KBL-R		Rev A00
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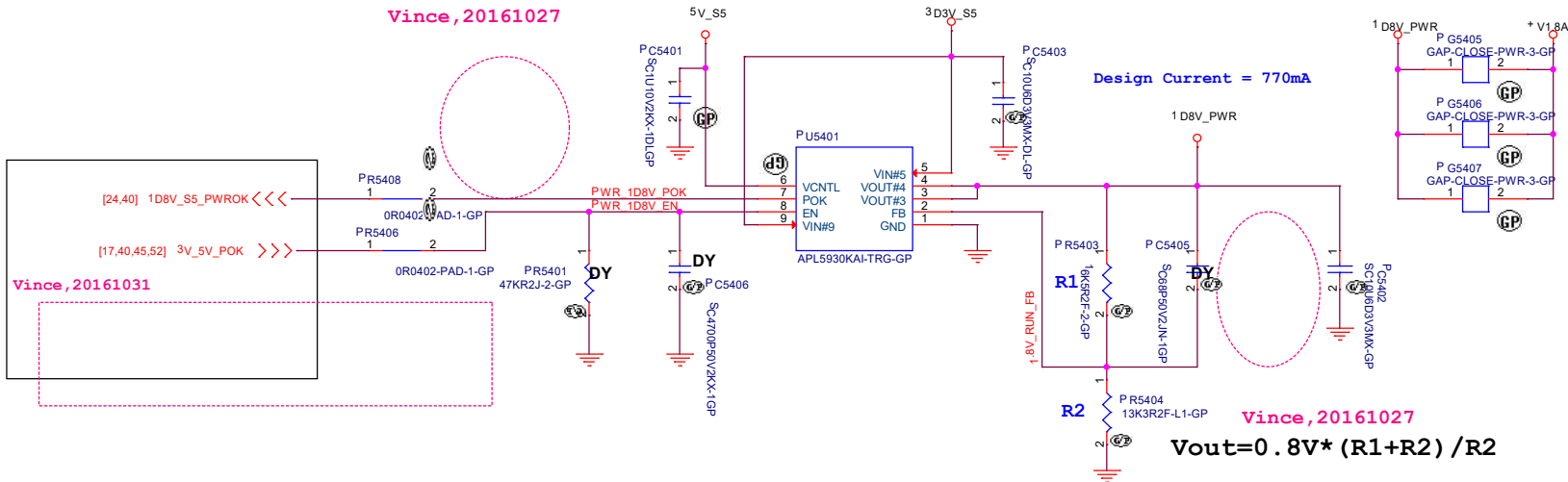
APL5930 for 2D5V



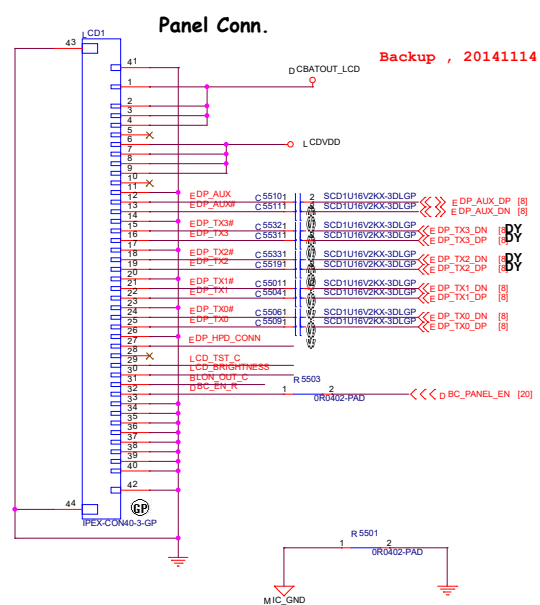
S-1339D15-M5001 for 1D5V_S0



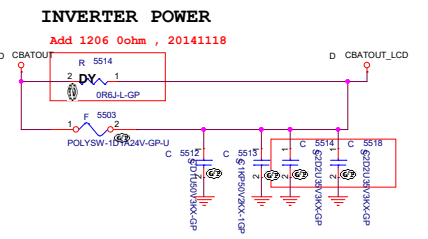
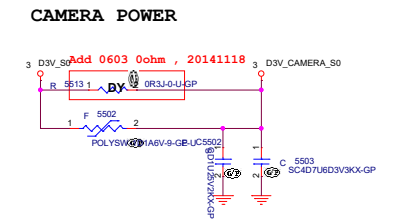
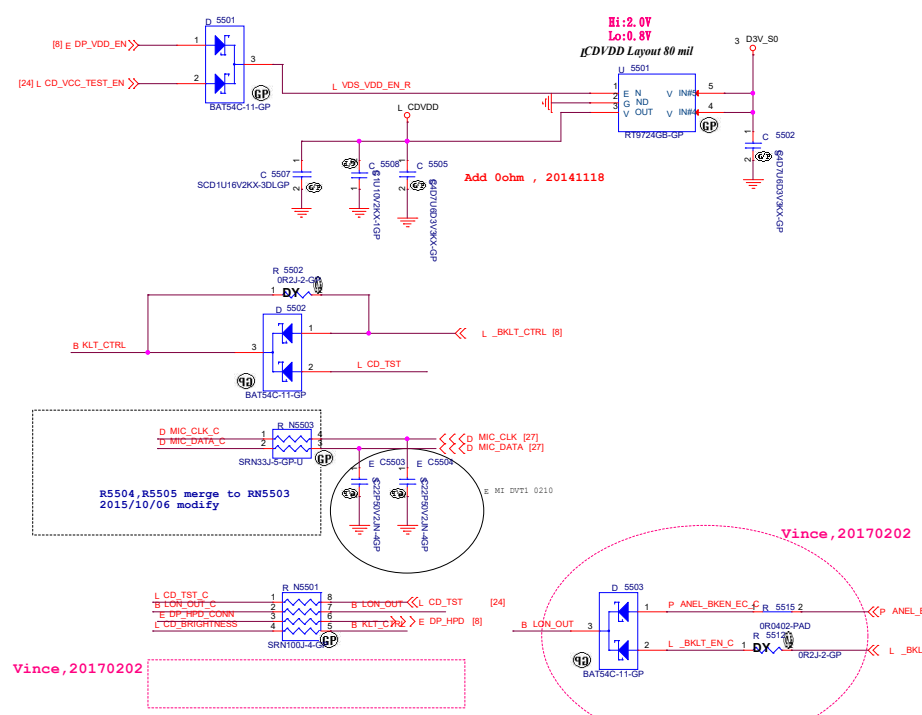
APL5930 for 1D8V_S5



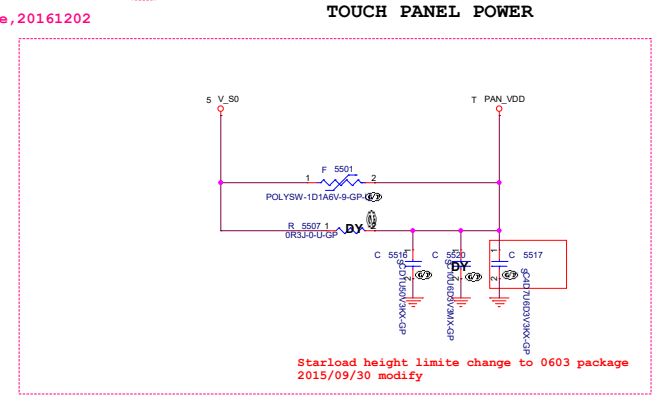
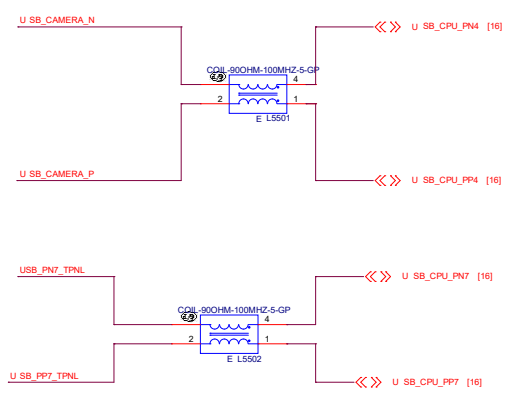
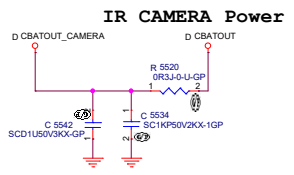
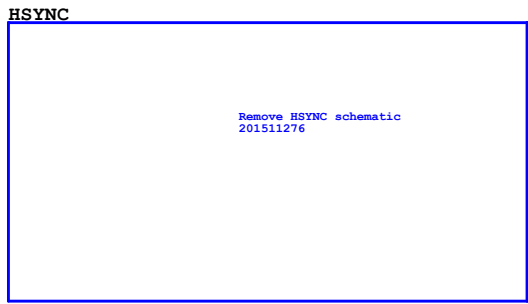
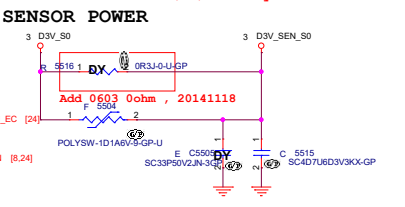
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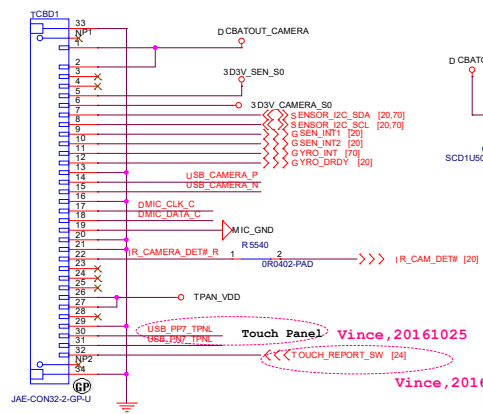
```
Power Pin Count : 7
GND Pin Count : 9
```



Starload height limite change to 0603 package
2015/09/24 modify



Starload height limite change to 0603 package
2015/09/30 modify



Touch Panel Vince,20161025
 <<< TOUCH_REPORT_SW [24]
 Vince,20161107

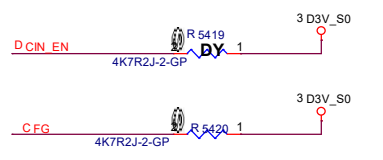
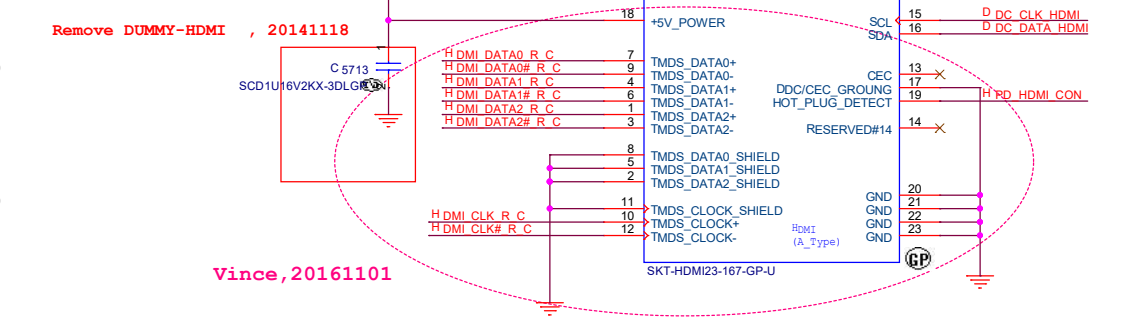
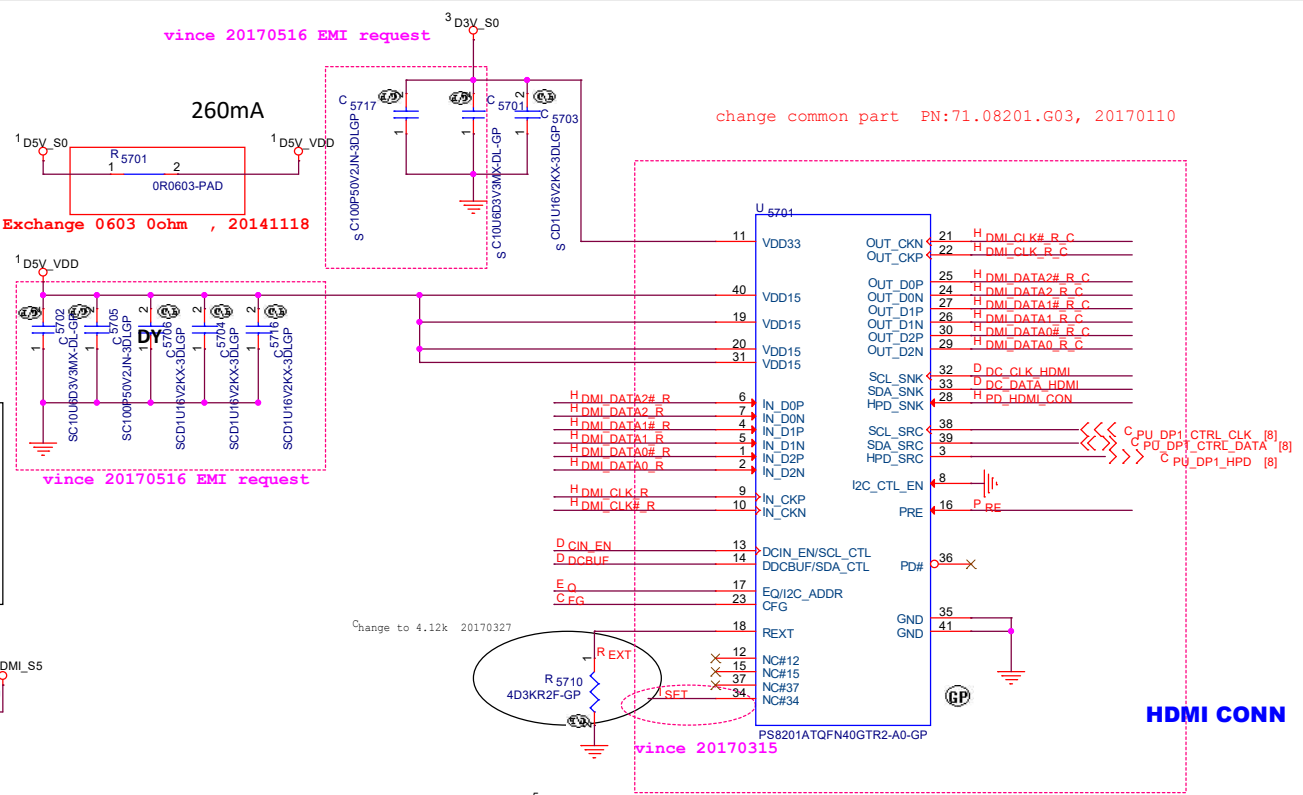
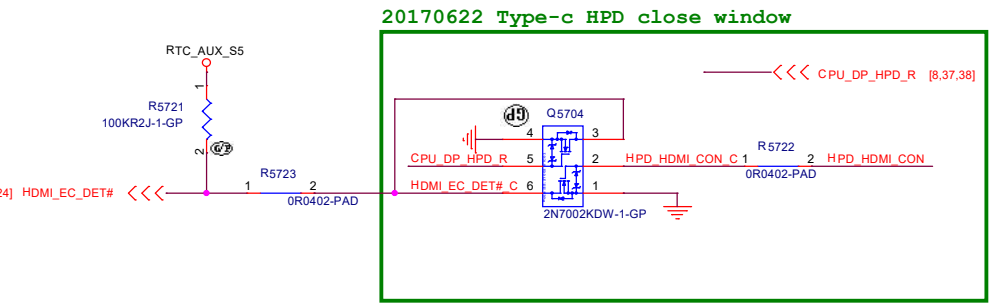
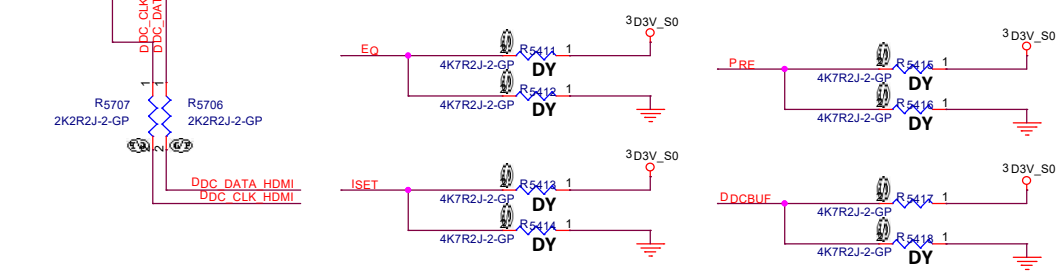
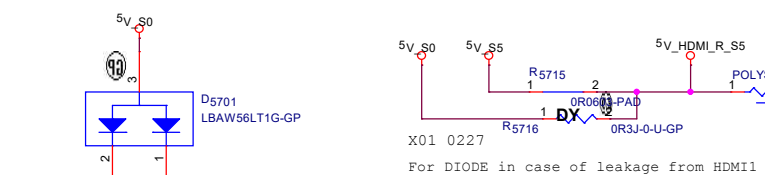
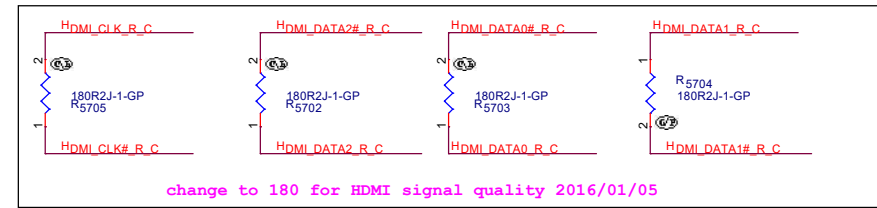
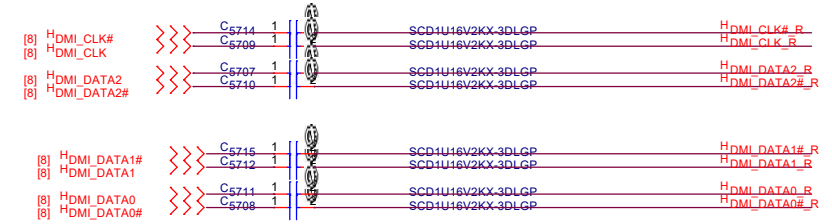
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CRT		
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SSID = HDMI



(Blanking)

<Core Design>



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Title

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Size

A 3

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<Core Design>



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A 3

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Main Func = ODD



Main Func = WLAN

<Core Design>

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Title			
NGFF WLAN CONN			
Size	Document Number		Rev
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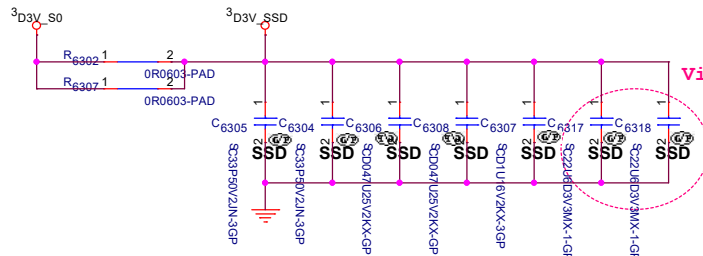
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Reserved			
Size A4	Document Number Starlord KBL-R		Rev A 00
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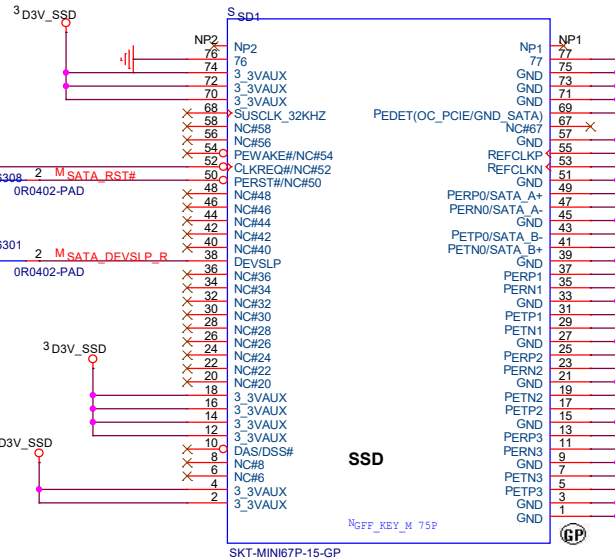
SSD = M.2

Vince, 20160929

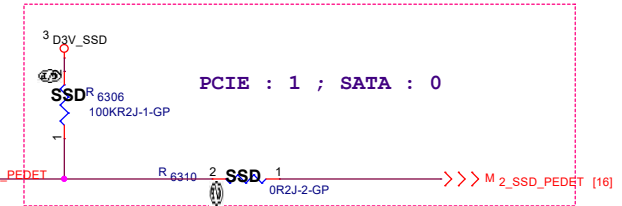


Vince, 20161028

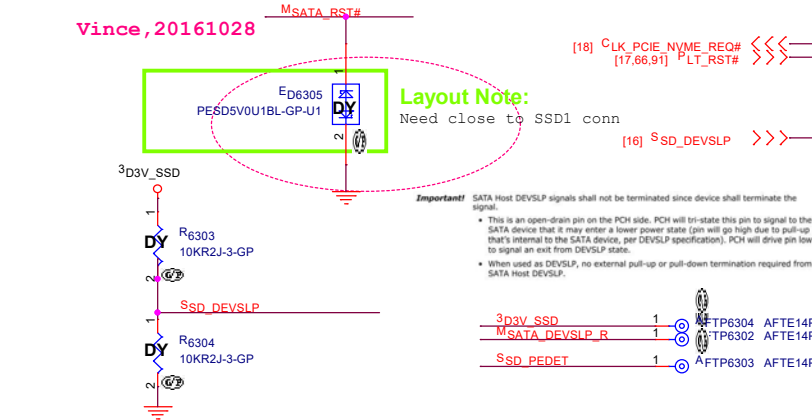
SSD M.2 CONN



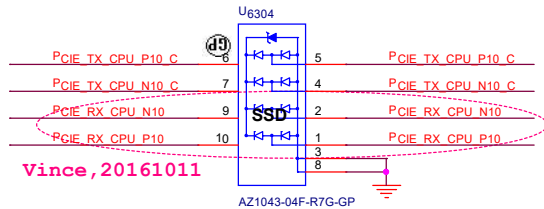
Vince, 20161103



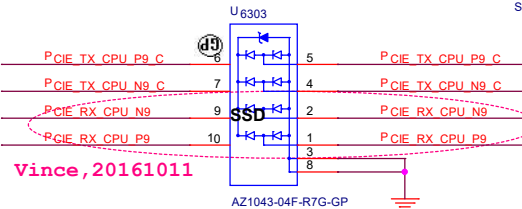
Vince, 20161028



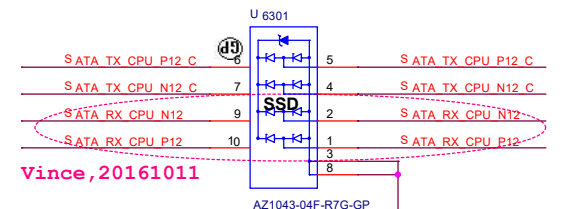
Layout Note:
Need close to SSD1 conn



Vince, 20161011



Vince, 20161011



Vince, 20161011

Table 13-12. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

Notes:

- Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.
- Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

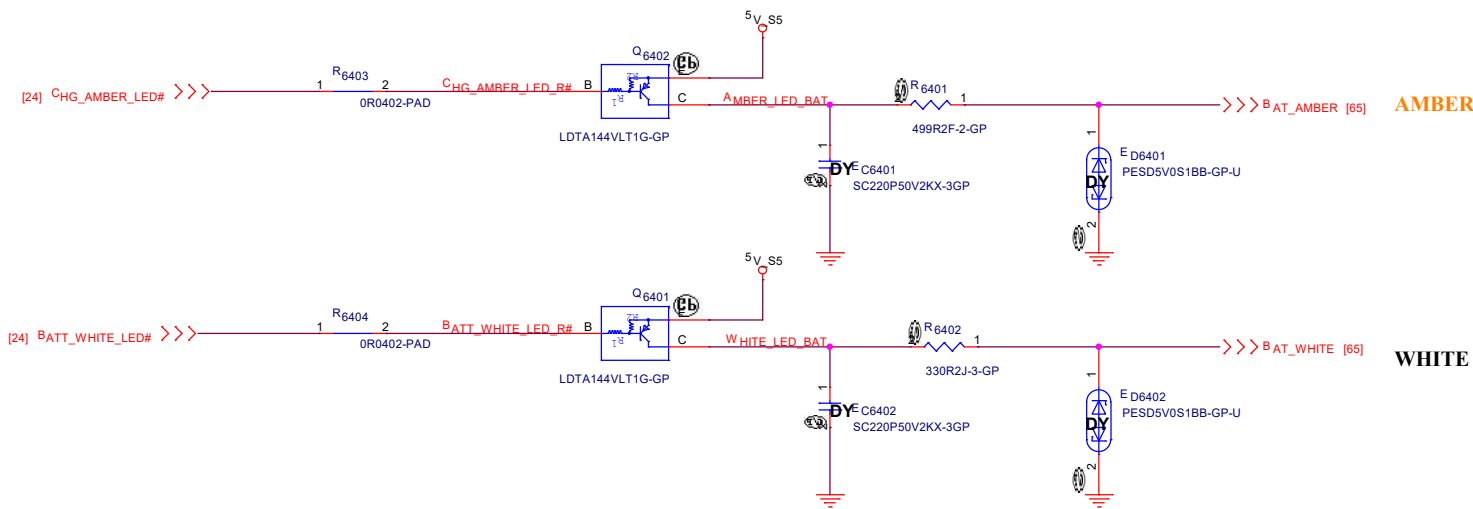
Pin	Signal	Pin	Signal	Pin	Signal
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2	3V3	12	NC	22	NC
3	3V3	13	NC	23	NC
4	3V3	14	NC	24	NC
5	3V3	15	NC	25	NC
6	3V3	16	NC	26	NC
7	3V3	17	NC	27	NC
8	3V3	18	NC	28	NC
9	3V3	19	NC	29	NC
10	3V3	20	NC	30	NC
11	3V3	21	NC	31	NC
12	3V3	22	NC	32	NC
13	3V3	23	NC	33	NC
14	3V3	24	NC	34	NC
15	3V3	25	NC	35	NC
16	3V3	26	NC	36	NC
17	3V3	27	NC	37	NC
18	3V3	28	NC	38	NC
19	3V3	29	NC	39	NC
20	3V3	30	NC	40	NC
21	3V3	31	NC	41	NC
22	3V3	32	NC	42	NC
23	3V3	33	NC	43	NC
24	3V3	34	NC	44	NC
25	3V3	35	NC	45	NC
26	3V3	36	NC	46	NC
27	3V3	37	NC	47	NC
28	3V3	38	NC	48	NC
29	3V3	39	NC	49	NC
30	3V3	40	NC	50	NC
31	3V3	41	NC	51	NC
32	3V3	42	NC	52	NC
33	3V3	43	NC	53	NC
34	3V3	44	NC	54	NC
35	3V3	45	NC	55	NC
36	3V3	46	NC	56	NC
37	3V3	47	NC	57	NC
38	3V3	48	NC	58	NC
39	3V3	49	NC	59	NC
40	3V3	50	NC	60	NC
41	3V3	51	NC	61	NC
42	3V3	52	NC	62	NC
43	3V3	53	NC	63	NC
44	3V3	54	NC	64	NC
45	3V3	55	NC	65	NC
46	3V3	56	NC	66	NC
47	3V3	57	NC	67	NC
48	3V3	58	NC	68	NC
49	3V3	59	NC	69	NC
50	3V3	60	NC	70	NC
51	3V3	61	NC	71	NC
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54	3V3	64	NC	74	NC
55	3V3	65	NC	75	NC
56	3V3	66	NC	76	NC
57	3V3	67	NC	77	NC
58	3V3	68	NC	78	NC
59	3V3	69	NC	79	NC
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61	3V3	71	NC	81	NC
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63	3V3	73	NC	83	NC
64	3V3	74	NC	84	NC
65	3V3	75	NC	85	NC
66	3V3	76	NC	86	NC
67	3V3	77	NC	87	NC
68	3V3	78	NC	88	NC
69	3V3	79	NC	89	NC
70	3V3	80	NC	90	NC
71	3V3	81	NC	91	NC
72	3V3	82	NC	92	NC
73	3V3	83	NC	93	NC
74	3V3	84	NC	94	NC
75	3V3	85	NC	95	NC
76	3V3	86	NC	96	NC
77	3V3	87	NC	97	NC
78	3V3	88	NC	98	NC
79	3V3	89	NC	99	NC
80	3V3	90	NC	100	NC

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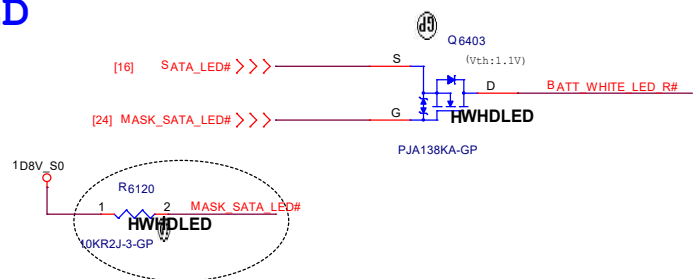
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Size A3	Document Number	Rev A00
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Battery LED1 (AMBER_LED)
Low actived from KBC GPIO



Battery LED2 (WHITE_LED)
Low actived from KBC GPIO

SATA LED



Add SATA LED solution by customer request 2016/02/03

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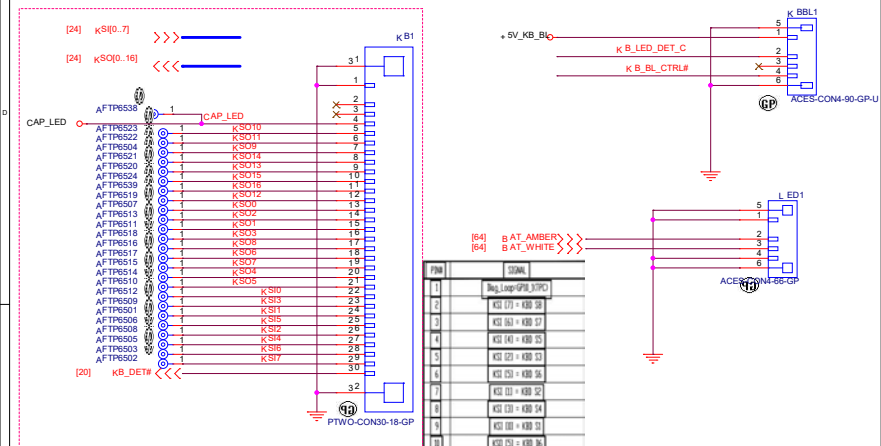
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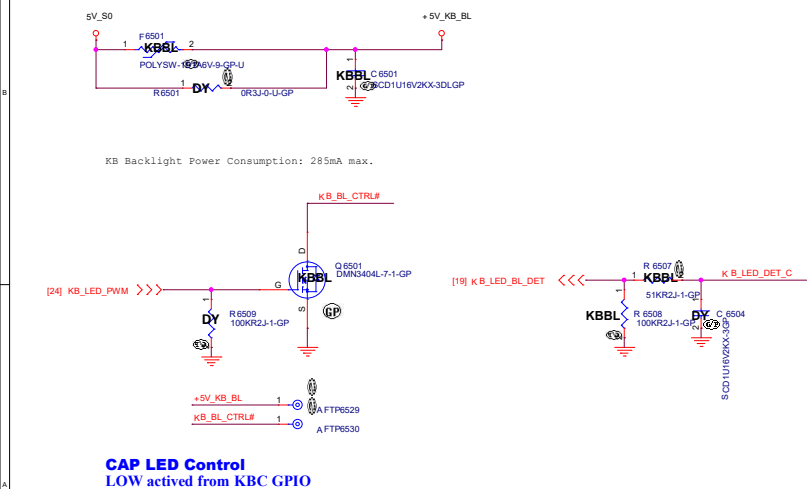
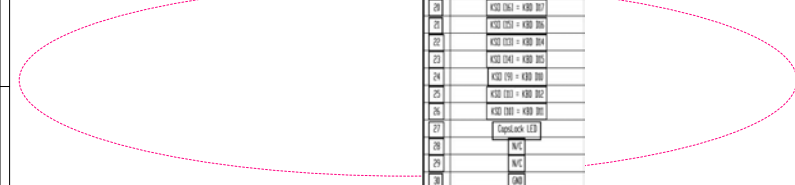
SSID = KB

Vince, 20170208

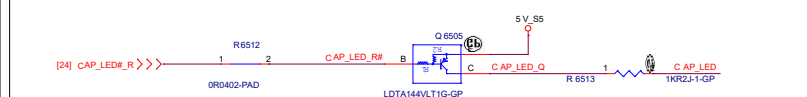
Keyboard



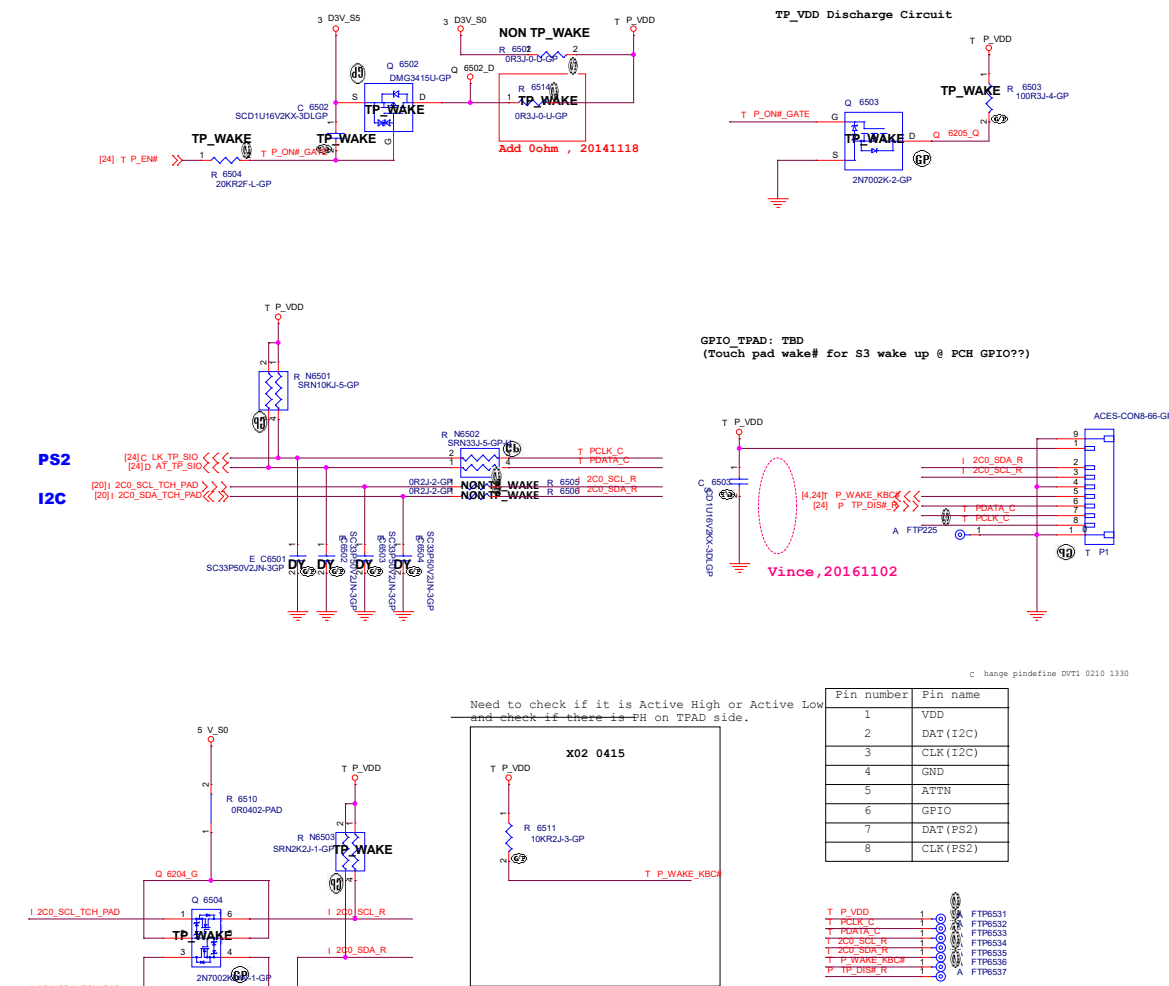
Vince, 20161201



CAP LED Control
LOW acted from KBC GPIO



Main Func = TPAD

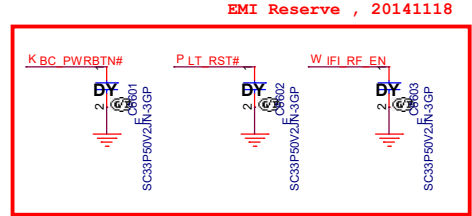
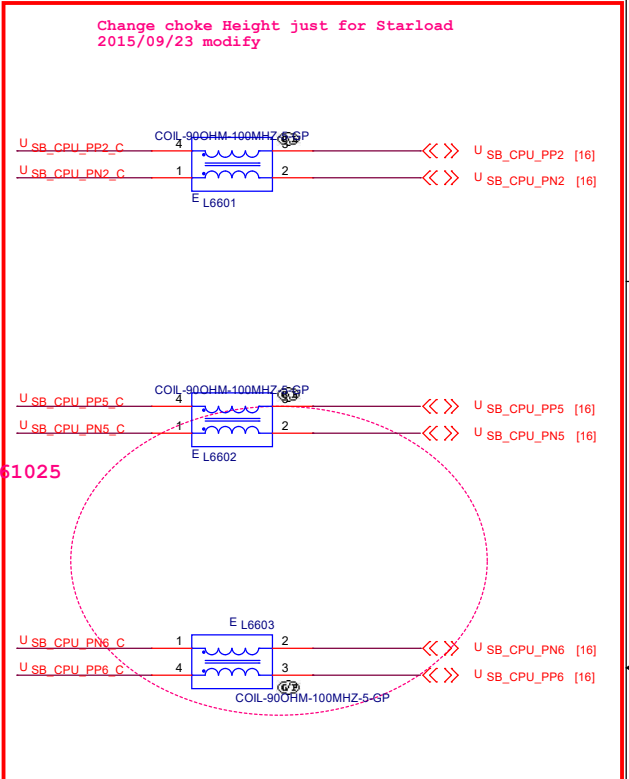
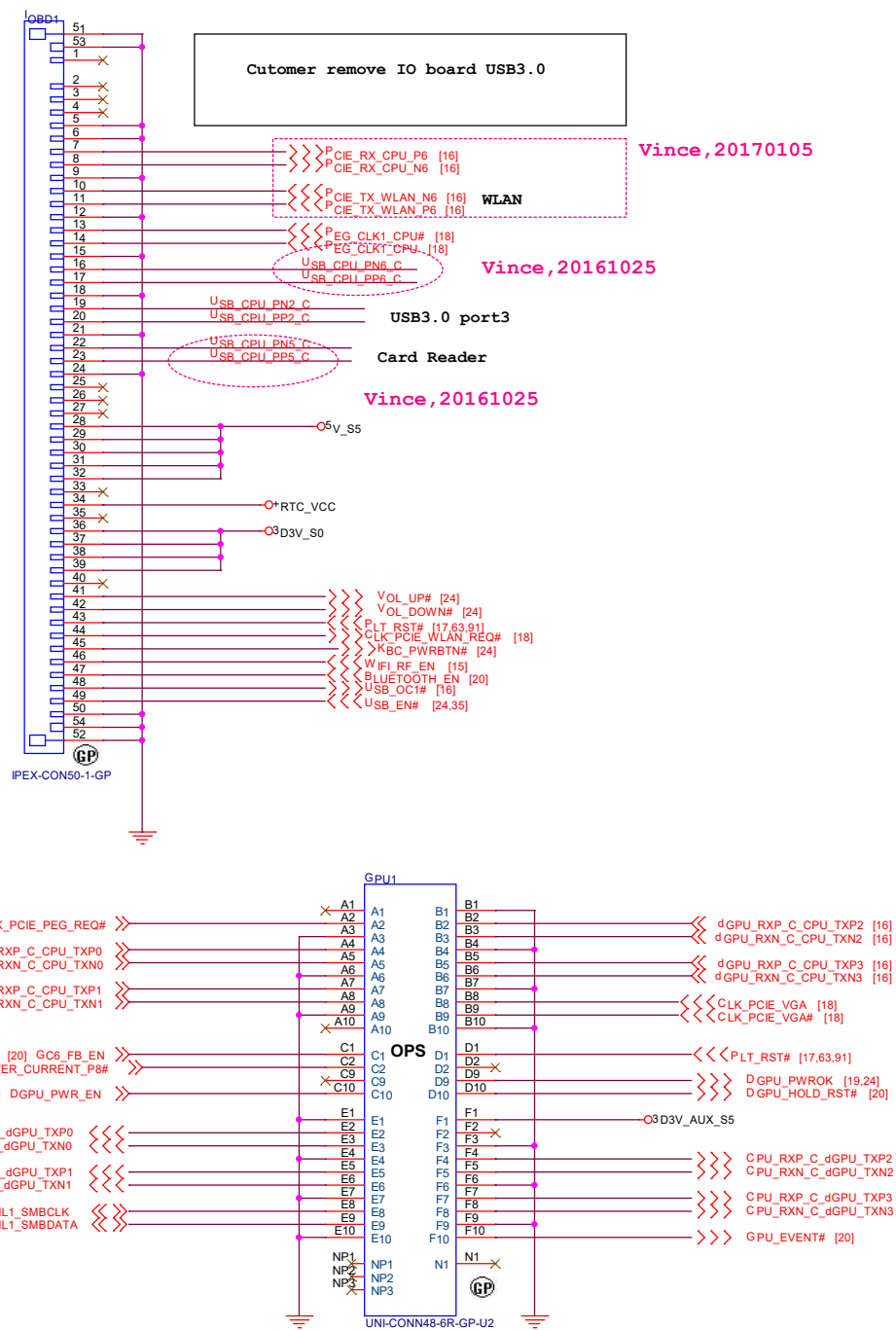


Need to check if it is Active High or Active Low
and check if there is PH on TPAD side.

Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	ATTN
6	GPIO
7	DAT (FS2)
8	CLK (FS2)

<Core Design>

SSID = IO Connector



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Title: **IO Board Connector**

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<Core Design>



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Title

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Document Number
Starlord KBL-R

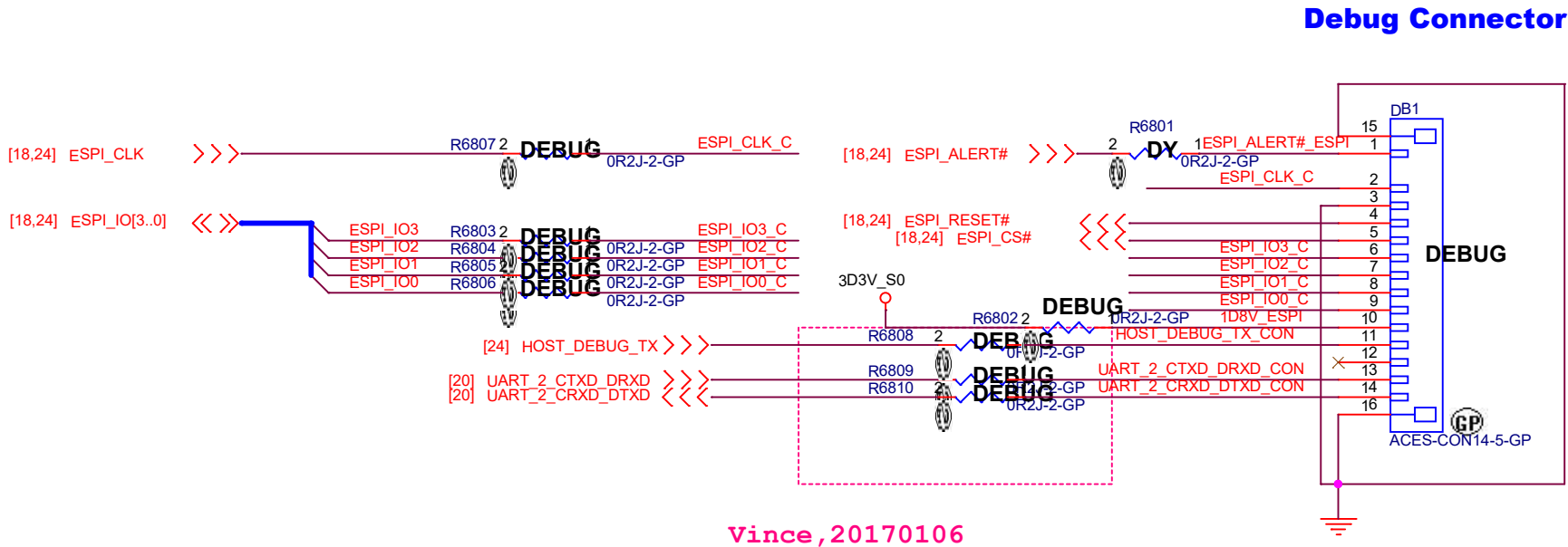
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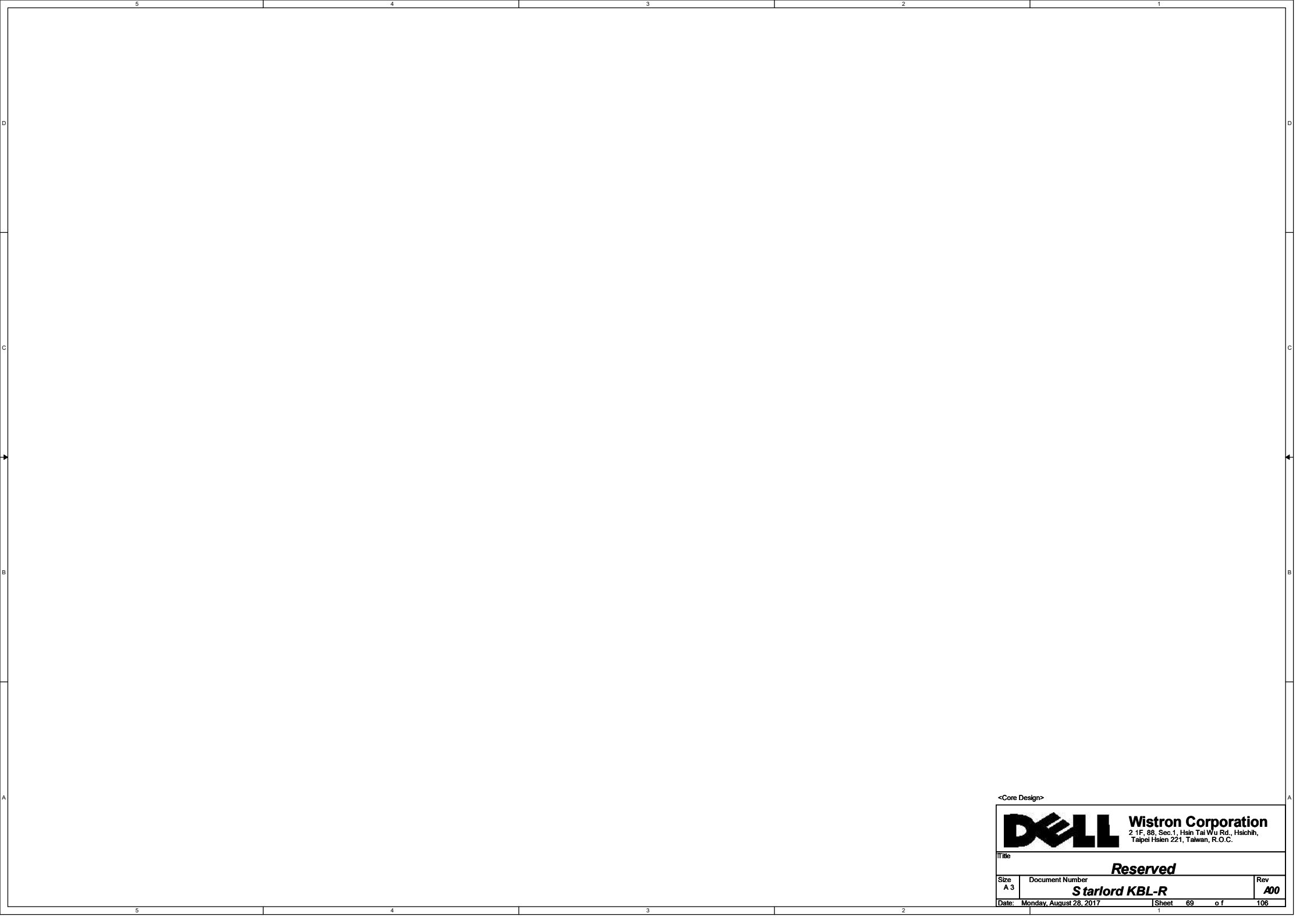
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SSID = Debug



<Core Design>

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Title			
Dubug connector			
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Title

USB3.0 PORT

Size
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Main Func = dGPU

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GPU(1/5)PEG

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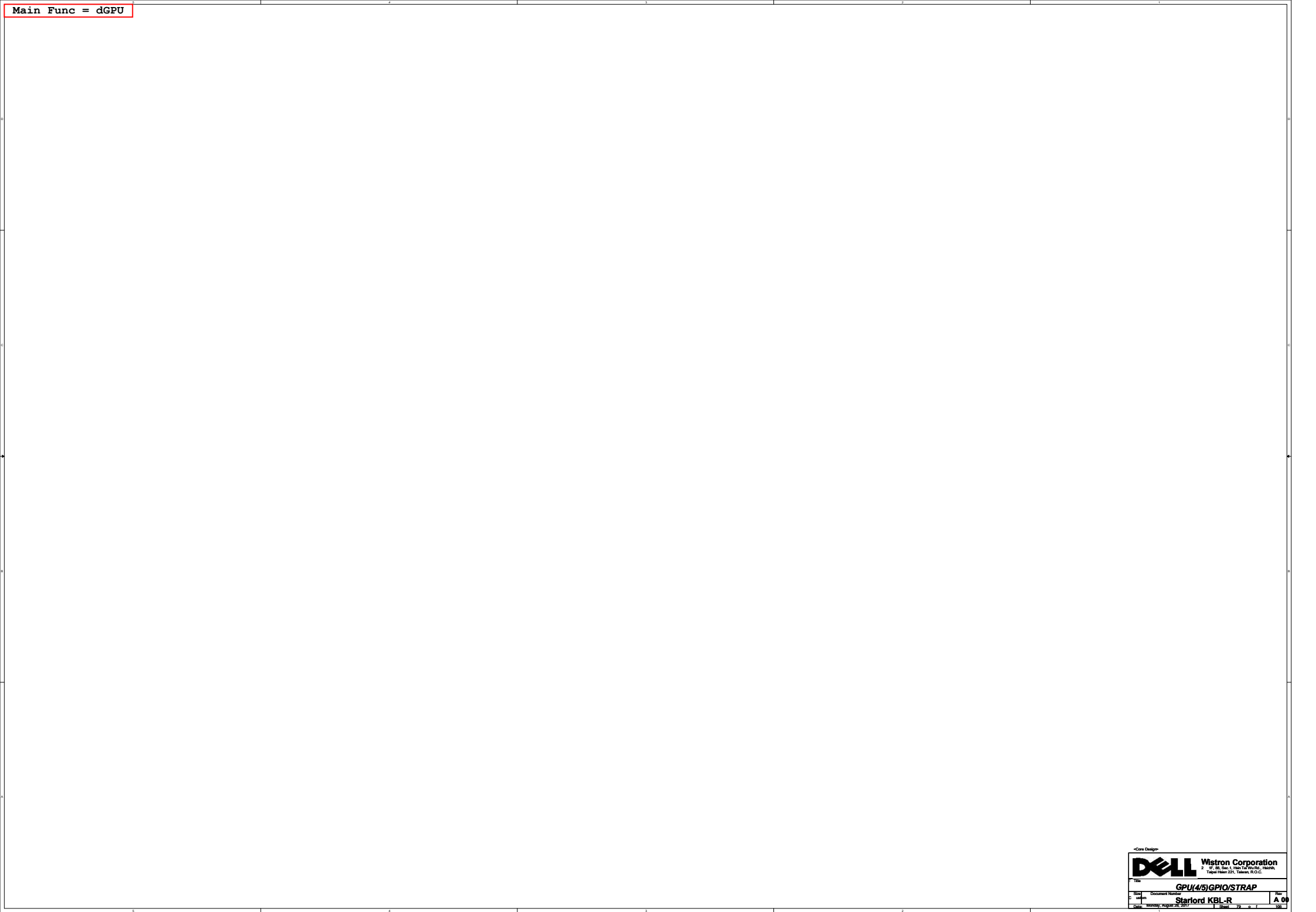
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GPU(5/5)PWR/GND

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GPU-VRAM3,4 (2/4)

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GPU-VRAM5,6 (3/4)

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GPU-VRAM7,8 (4/4)

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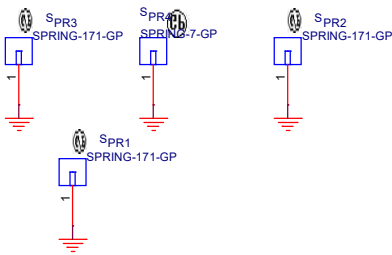
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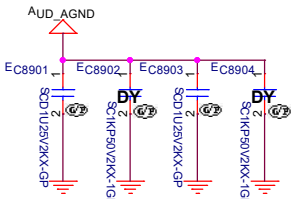
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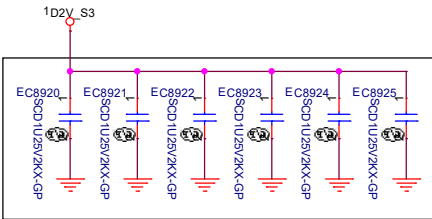


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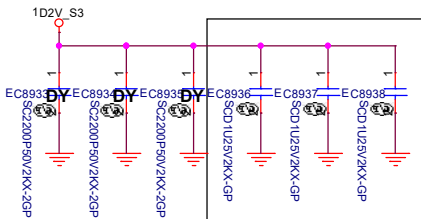
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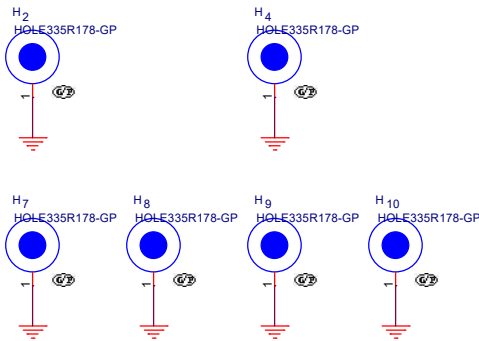


Change to 0.1uF at 20150427 for EMI

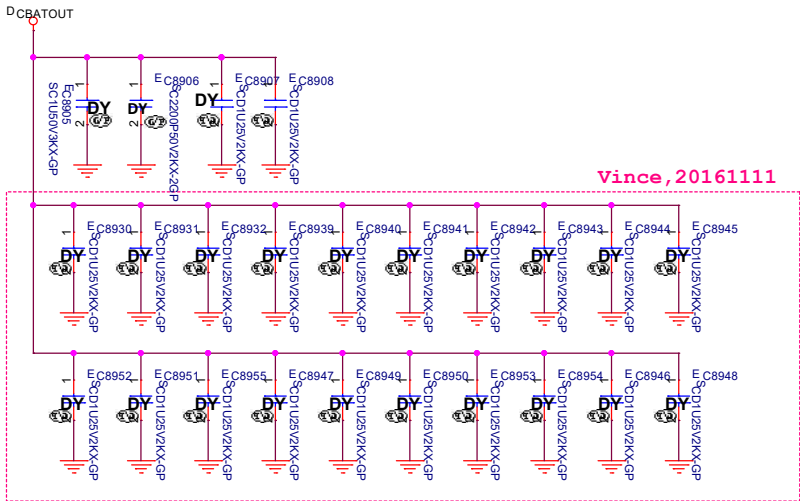
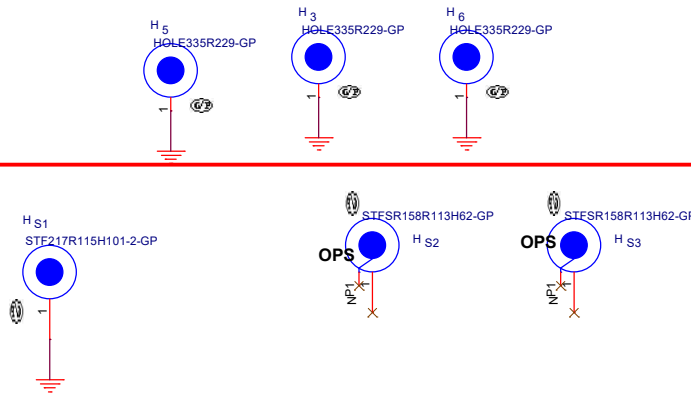


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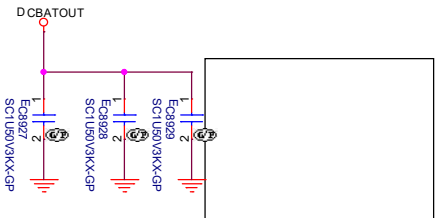
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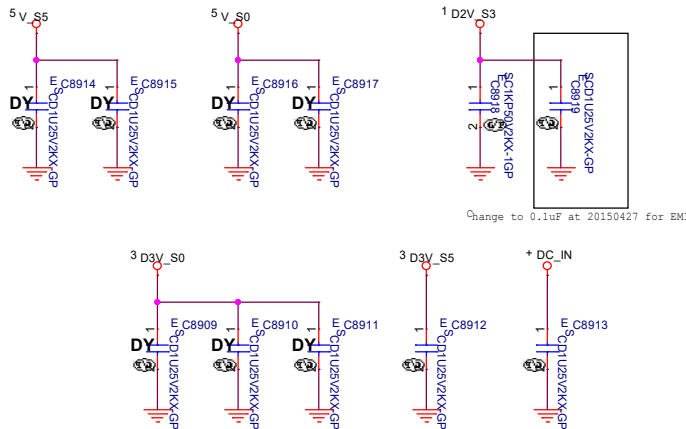
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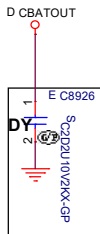
Vince, 20161111



Remove EC8931, EC8932, EC8926, EC8930 for placement



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RF request 2016/01/12 modify

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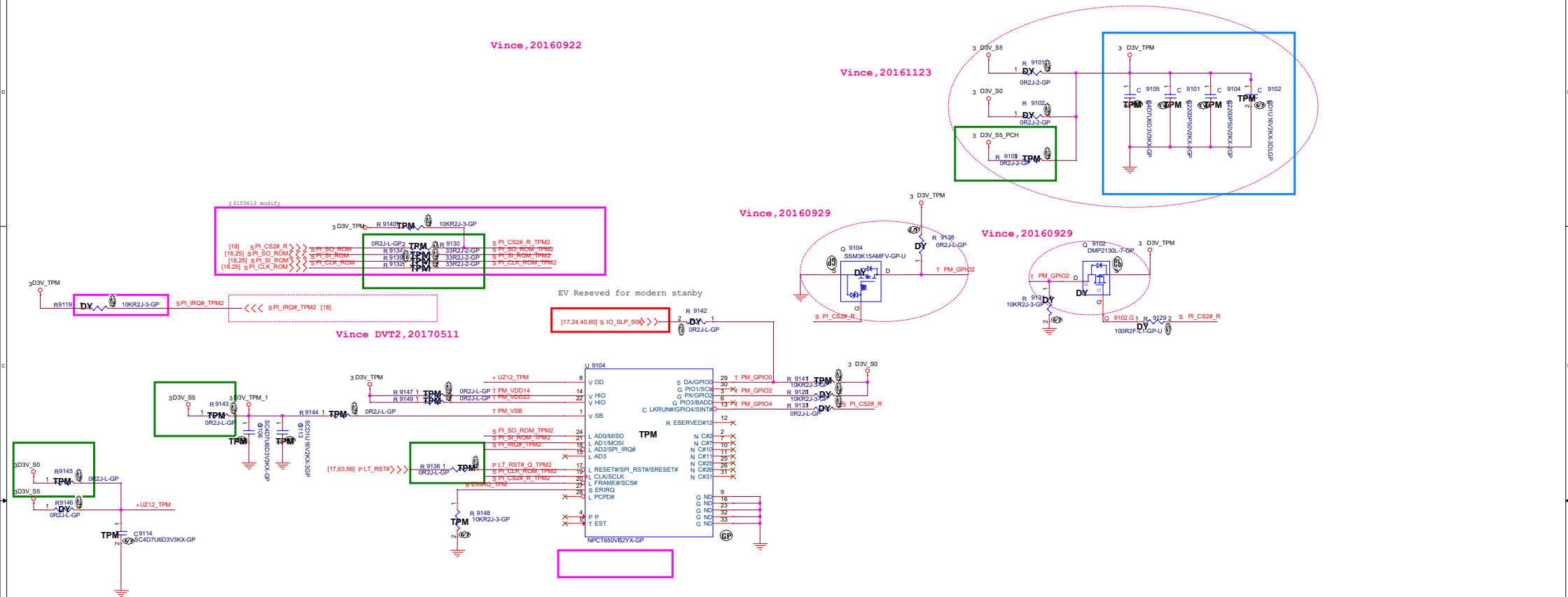
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SSID = TPM



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LVDS_Switch

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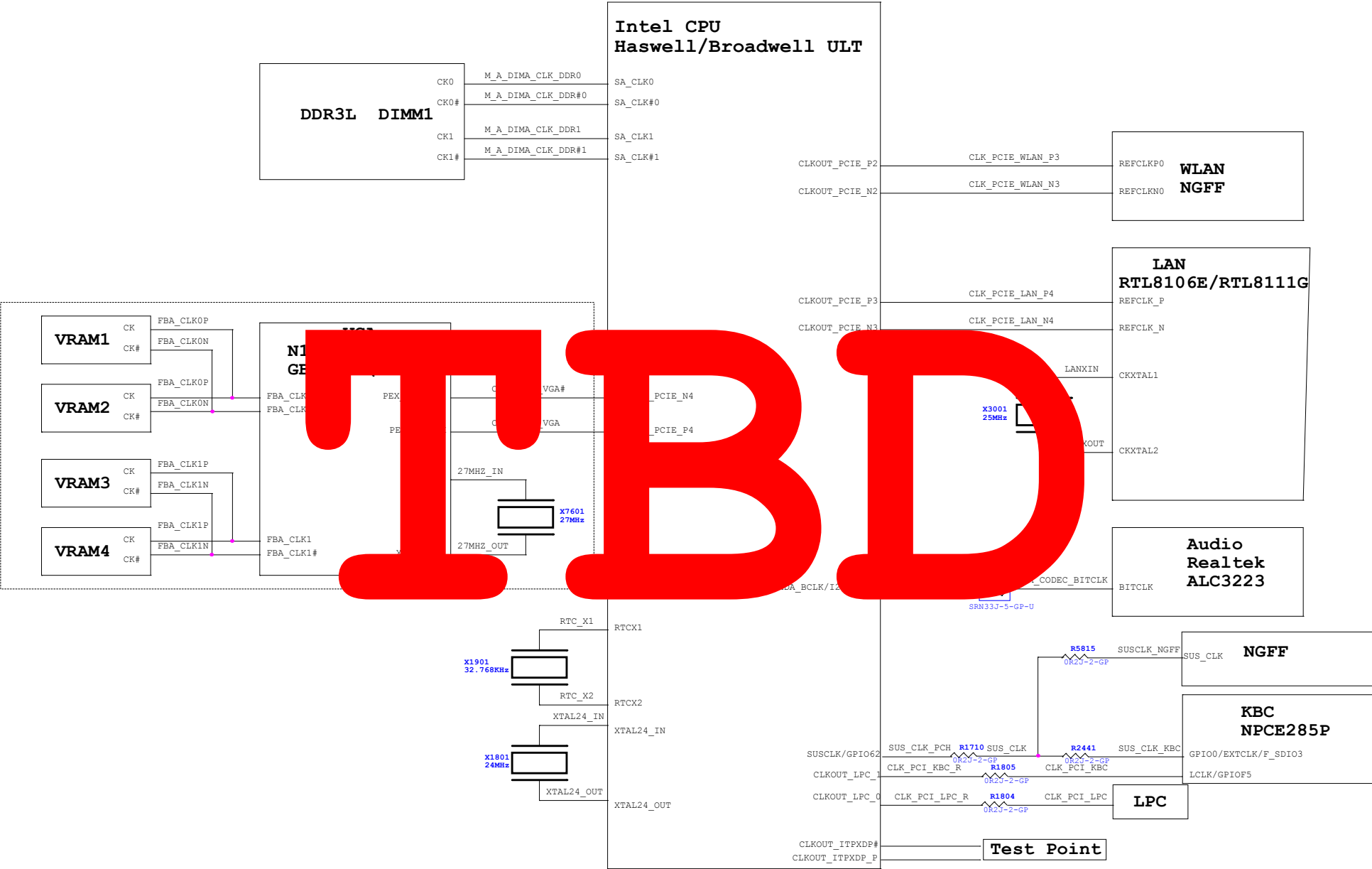
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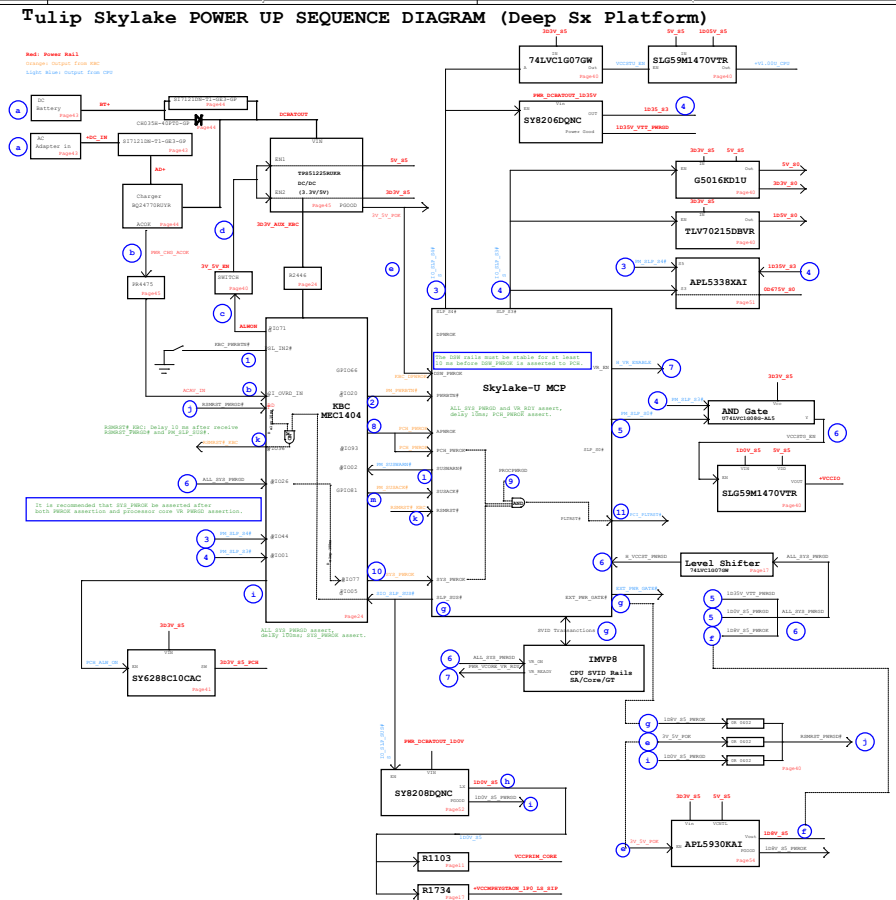
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Title CPU_XDP:PCH_XDP			
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CLK Block Diagram



[illegible][illegible]



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Note:

- The ramp time for any rail must be more than 40 ns and is recommended to be less than 2ms.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- The previous power rail must ramp up to 90% before the next power rail can start ramping up.
- No signal should be applied to the GPU before the power rails are fully ramped.
- Refer to the JEDEC Memory Specification for memory related power sequencing.
- The order of NVDD and PEX_VDD ramp-up can be reversed during GCA exit, when there is a back-to-back GCA entry/exit and/or when PEX_VDD takes longer to ramp down/during GCA entry.

There is no specific power down sequence. However, residual voltage from power down must not violate the power-up sequence when back to back GPU power-down and power-up events take place.

The following timing diagram in Figure 18-12 and Table 18-3 describes the GC6 2.0e exit sequence and timing requirements.



Figure 18-12. GC6 2.0 Entry/Exit Sequence Timing Diagram

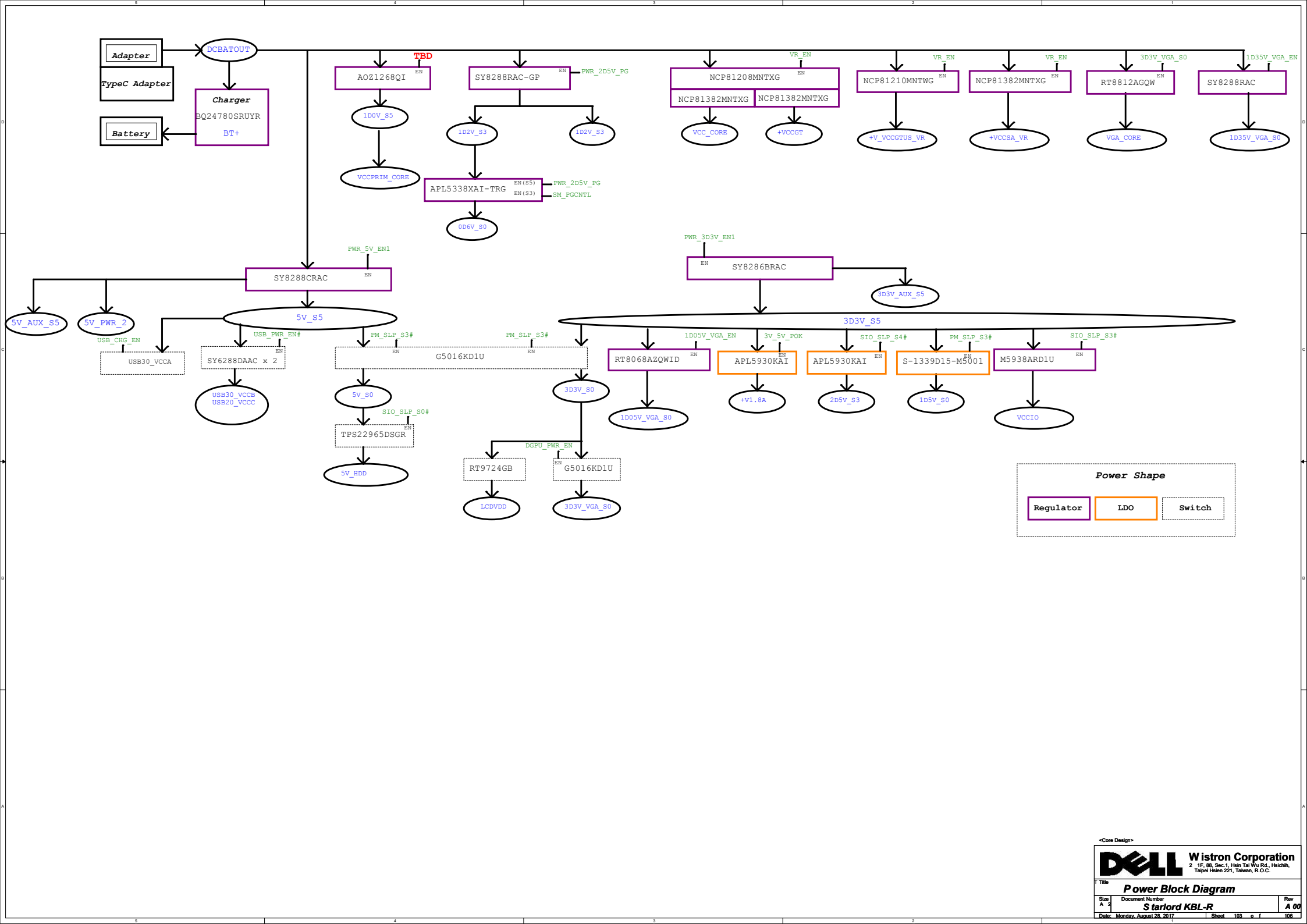
Table 18-2. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EHNT assertion period	0.001	N/A	ms
T1	3% VMAIN_EH assertion to all power rails up and stable	0.04	4	ms

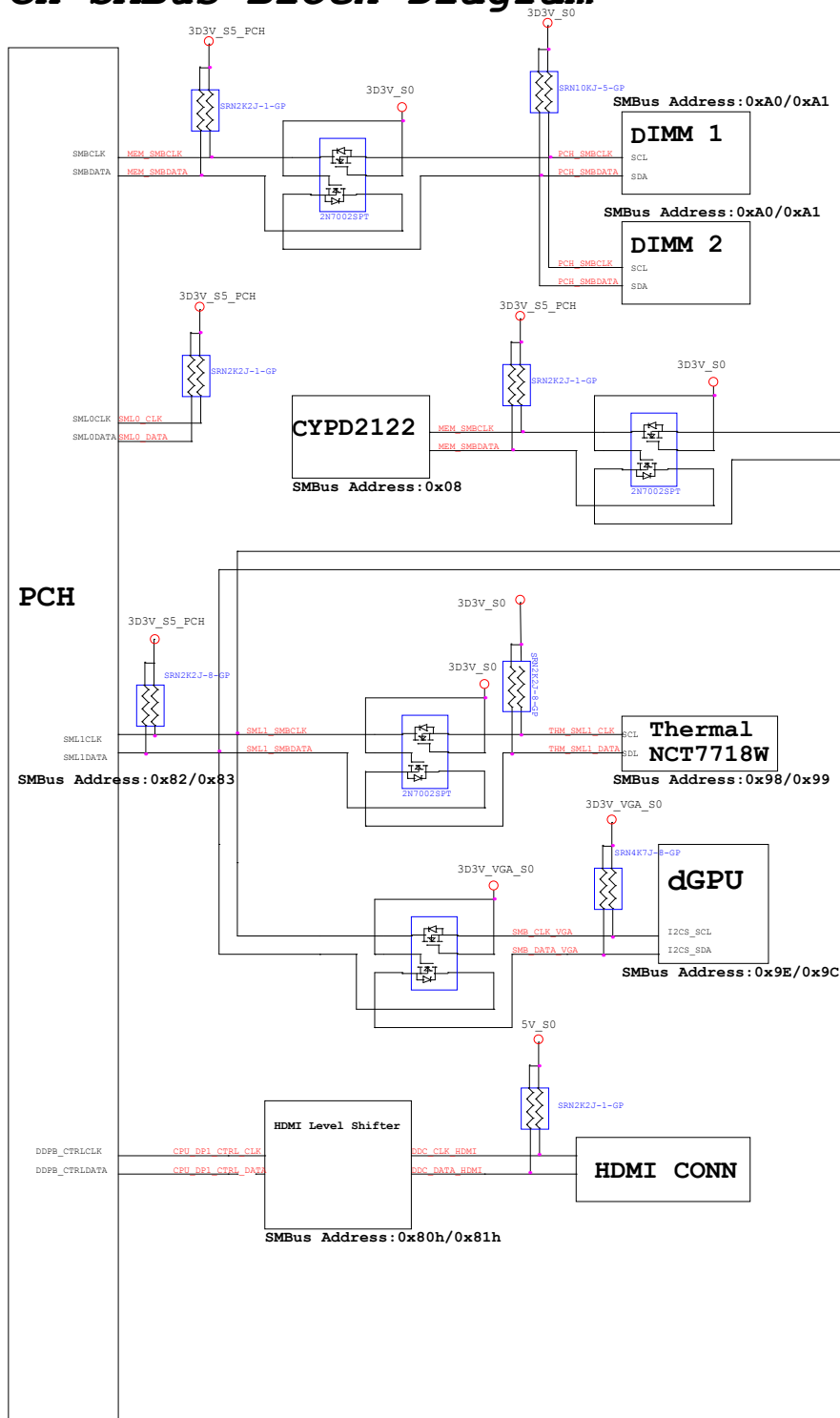
Winter

- All Pail PGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
- During GPU exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
- All delays should be minimized to increase time spent in G6s for maximum power saving.
- The entire entry/exit sequence must complete within 200 ms.

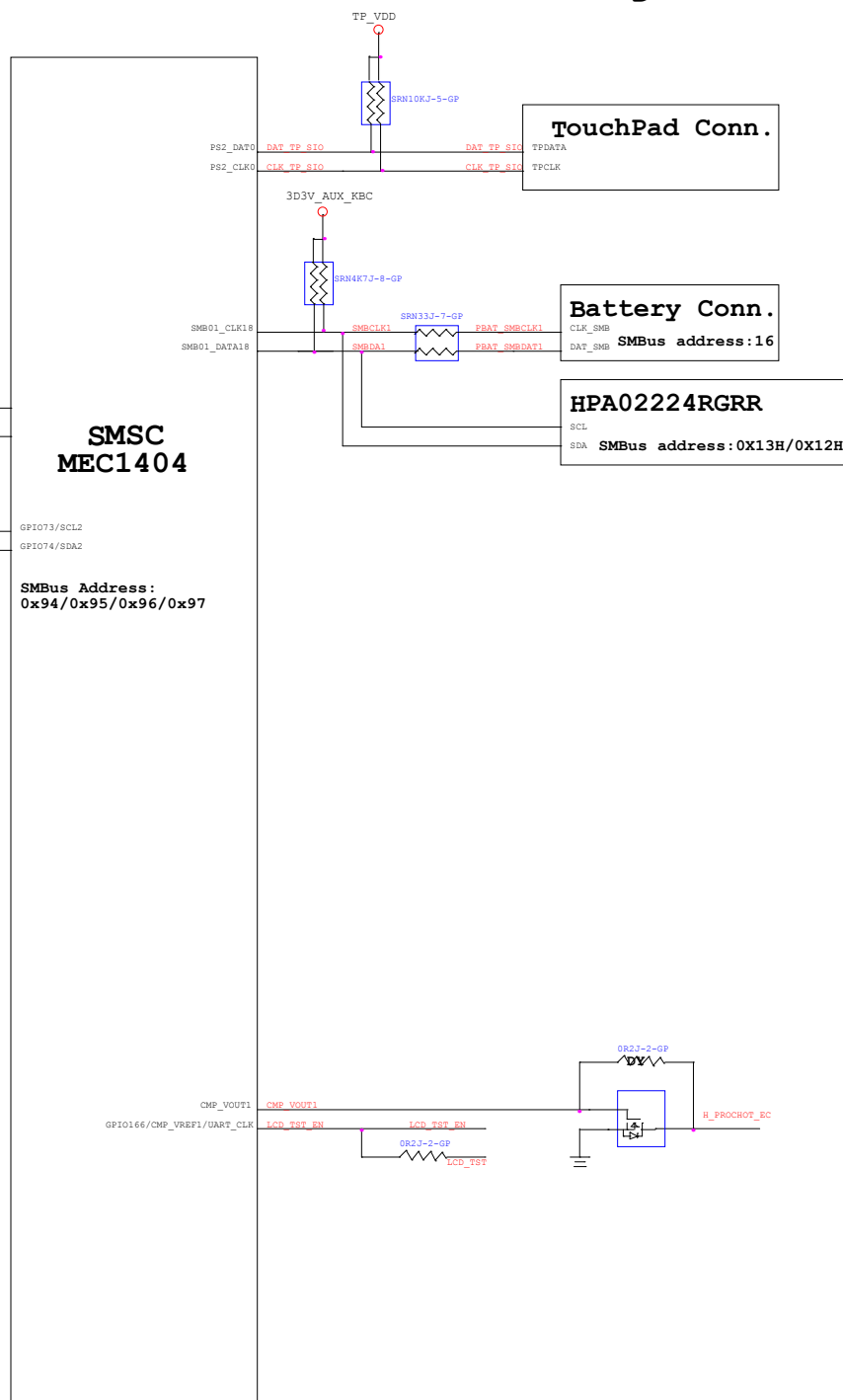




PCH SMBus Block Diagram

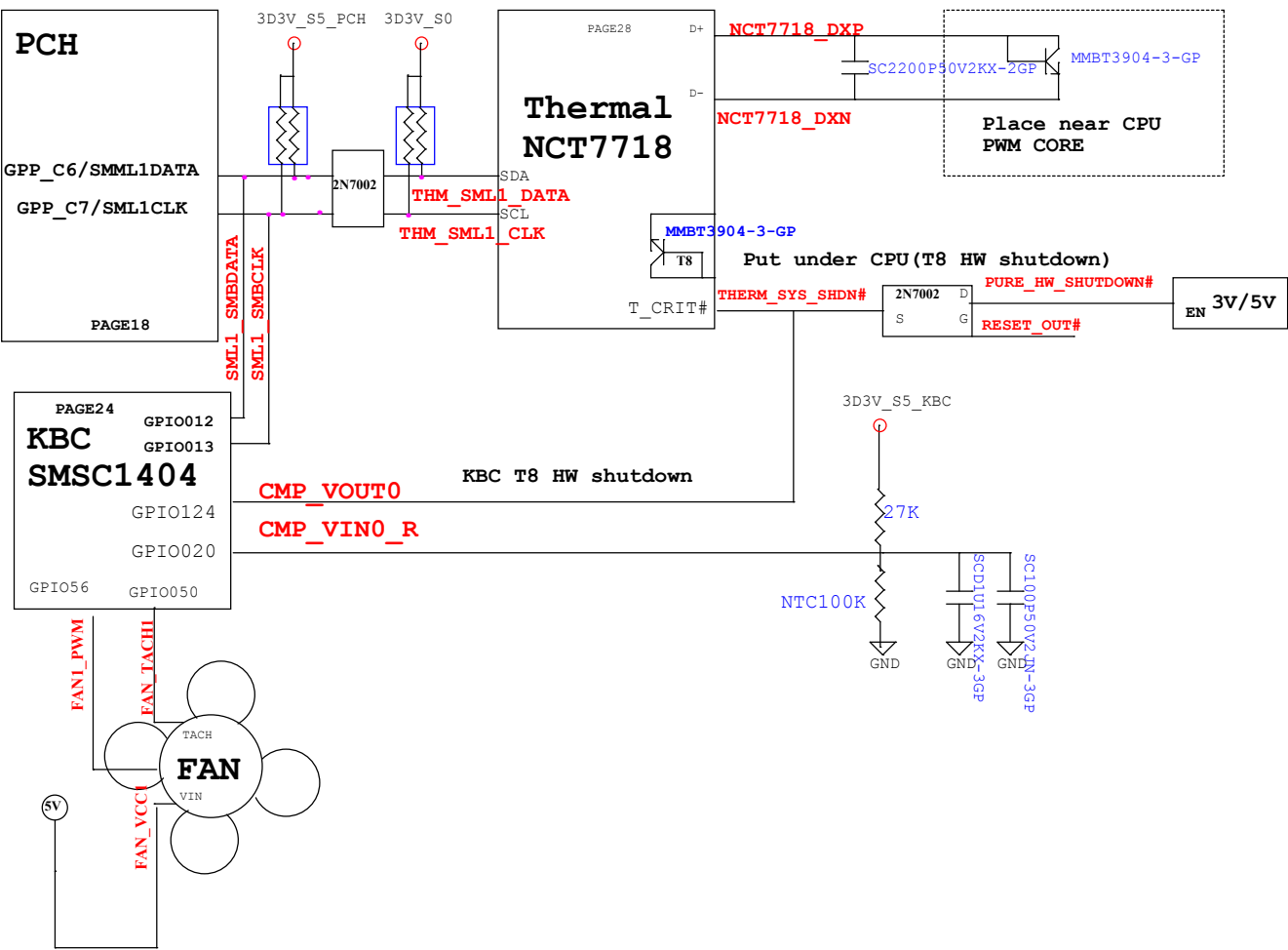


KBC SMBus Block Diagram

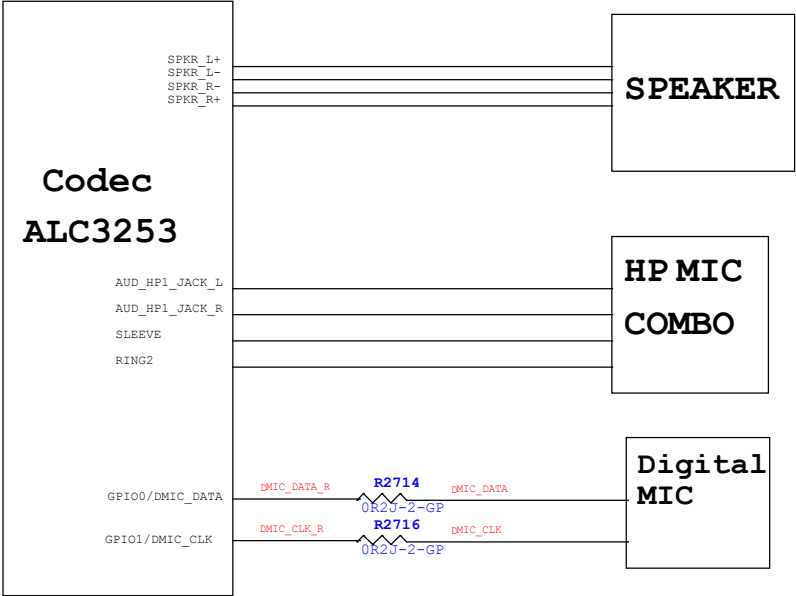


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Thermal Block Diagram



Audio Block Diagram



5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

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